How to get custom SoCs done fast and correct

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RISC-V IN SPACE

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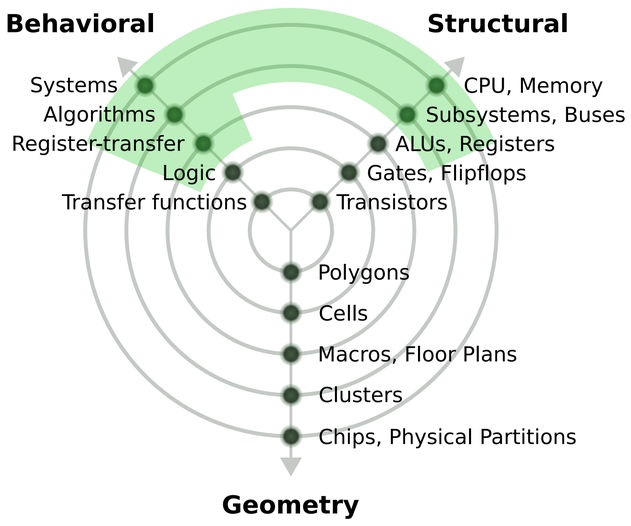
1. Introduction

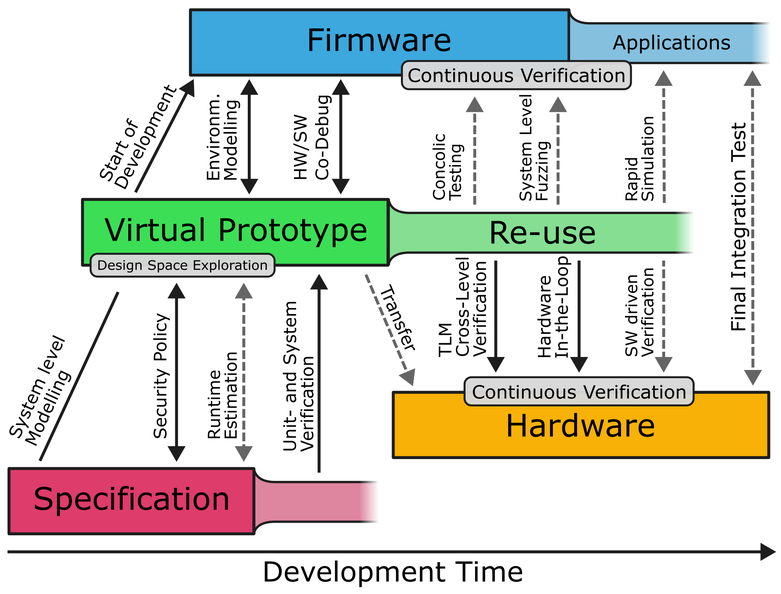
Virtual Prototypes (VPs) are incredibly useful for the complex *System on Chip* (**SoC**) design process. A VP creates the possibility to **design, evaluate and verify** an executable prototype of the system in an early design stage by modelling the future *Hardware* (HW) on an **system** / **architectural** level.

The VP-enhanced system design flow enables both the **iterative design evaluation** and **parallel development** of the (actual) HW and *Software* (SW) very early in the product conception phase. Additionally, VPs can be used as **golden reference models** with test and verification methods for comparison between the system level behaviour and the actual HW.

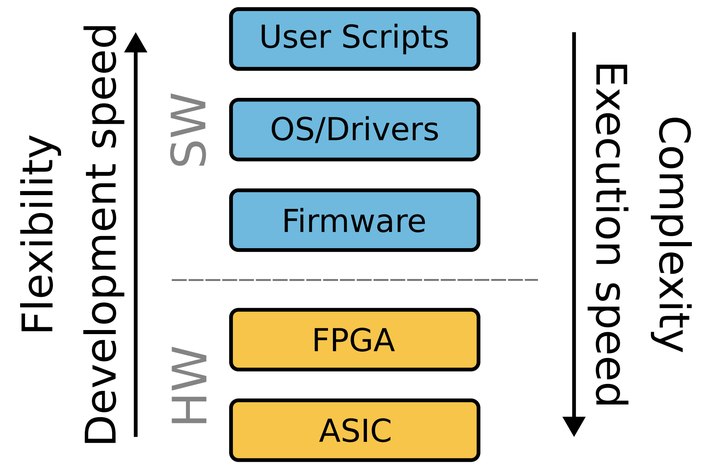


2. Process Speedup

The main goal of this poster is to encourage companies and individuals to use VPs and invest in the comparatively low effort to create a correctly configured VP to benefit from new possibilities. Most notably, to show improvements in **development speedup**, **SW quality**, **HW quality**, and **accessibility**.

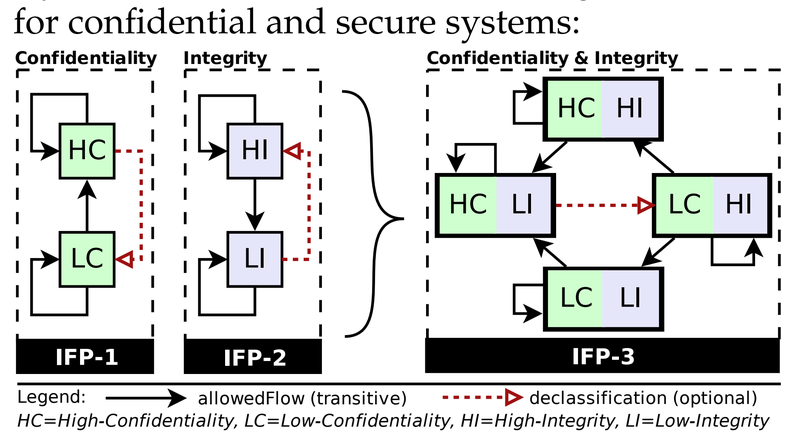


The speedup mainly relies on the **HW/SW co-development** (shift left principle) and **early design space exploration**. This allows problems like HW-SW-Partitioning [6] to be solved **before** the existing design can't be changed.

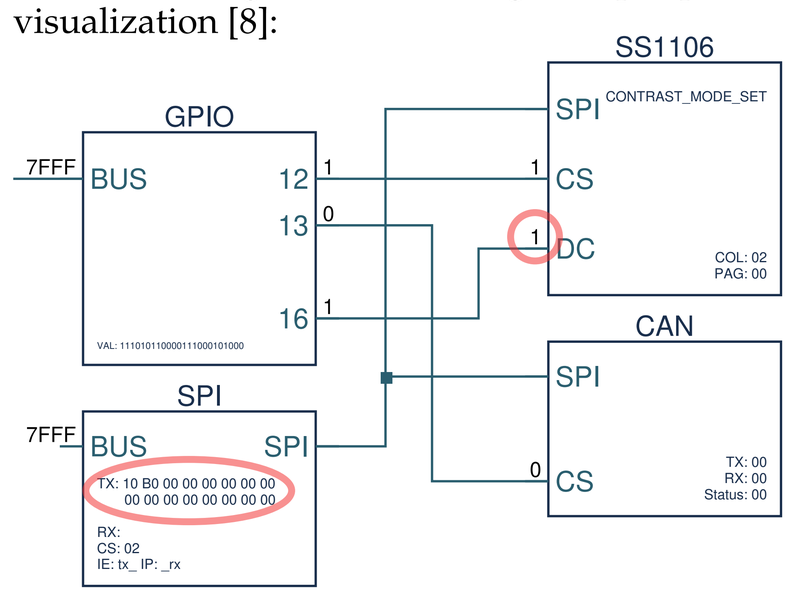


3. SW quality

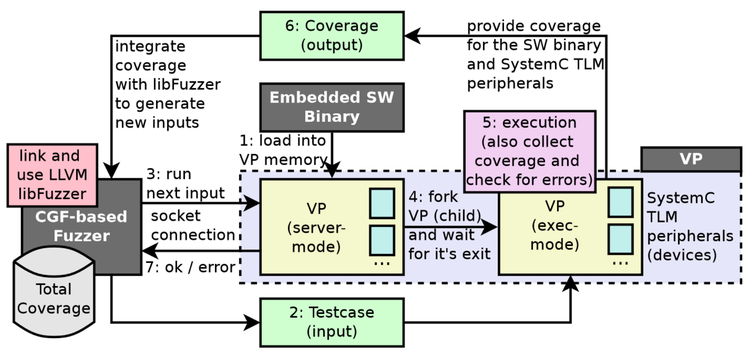
Dynamic Information Flow Tracking [7] for confidential and secure systems:



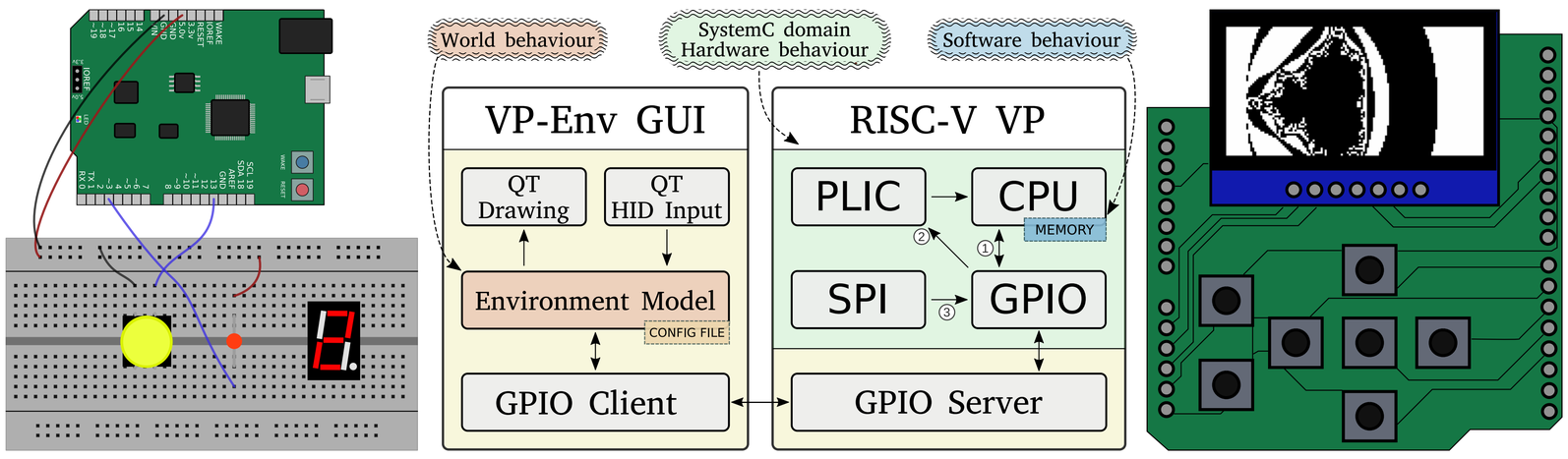
Firmware design understanding with peripheral visualization [8]:



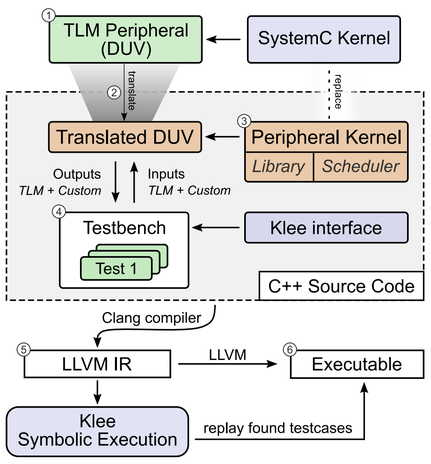
Symbolic and concolic execution of low-level SW that interacts with HW [9, 10, 11]:

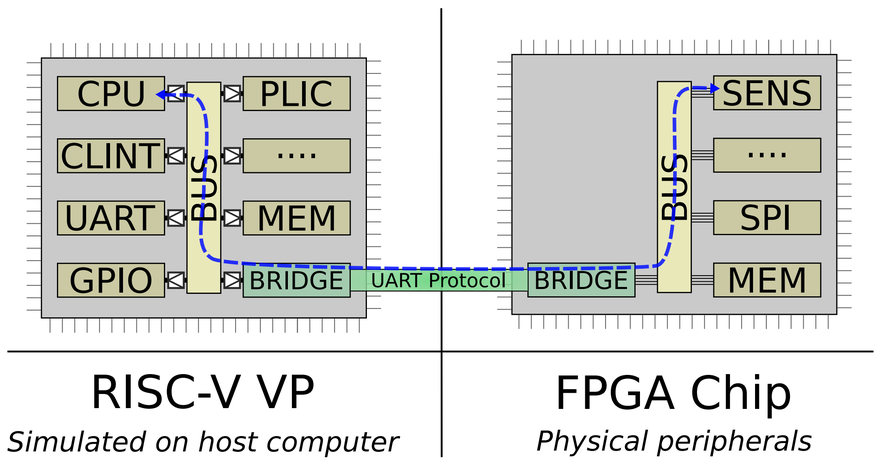


4. HW Modeling and Quality



- Interactive environment modeling [12] for off-chip devices on a PCB
- Constrained random verification [13] for HDL-vs-TLM comparison
- Symbolic execution of SystemC models [14], with HDL-synthesis methods [15]
- Hardware-in-the-Loop testing [16] or co-simulation [17] for focus on unique selling point





5. References

Sorted by execution speed vs. low-level detail: QEMU [1], RISC-V JIT [2], Renode [3] and TLM-based platforms such as the RISC-V VP [4, 5].

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