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FAST SINGLE EVENT UPSET DETECTION TECHNIQUE FOR PROCESSORS USING AN ALL-DIGITAL FLOW

ABSTRACT

This work presents a method for detecting single event transients and single event upsets in flip-flops immediately after they occur by using a double flip-flop sampling technique.
This technique does not involve any timing delay on the data path, making it useful for high performance and high reliability systems in space. These upsets can be reported at the processor to take further mitigation actions, such as roll-back

INTRODUCTION

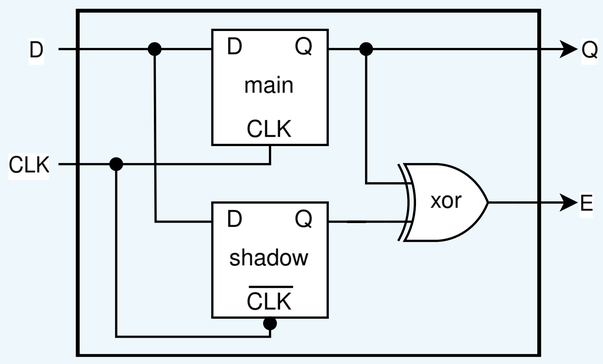
Single event transients (SETs) are induced by an ionizing particle. SETs cause temporary disturbances in combinatoric logic.

Single event upsets (SEUs) induced by SETs are captured on the active clock edge of sequential logic. SEU occurrence is proportional with the clock frequency.

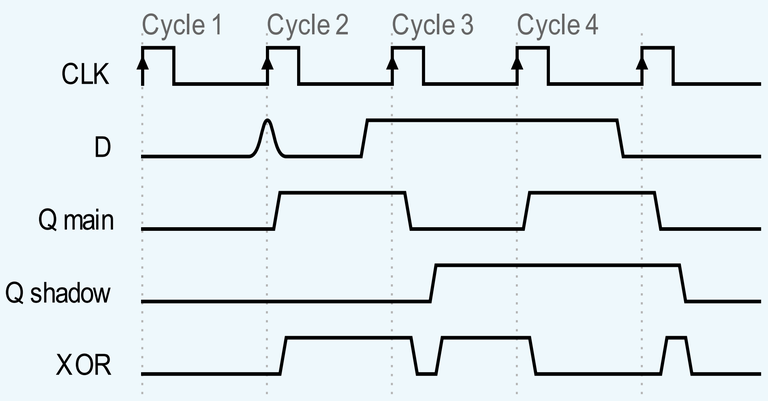
PRESENTED WORK

Detect SEUs inside a flip-flop and SETs arriving at a flip-flop.

Double Sampling Flip-Flop (DSFF)
Sample the data path twice and compare the results.
When the data input has changed within the time window between both samples, a SET has occurred in the combinatorial logic.



Schematic of a double-sampling flip-flop



Waveform of double-sampling flip-flop detecting single event upsets

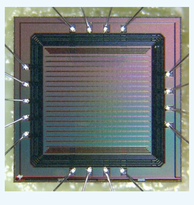
Benefits
- No additional delay is introduced in the data path.
- Full digital flow with only standard logic library cells.
- Interrupt controller from processor can handle the errors.

Considerations
- Timing needs to be properly constrained for half-cycle paths.

TEST RESULTS

The DSFFs were verified in silicon on 180 nm bulk cmos technology.

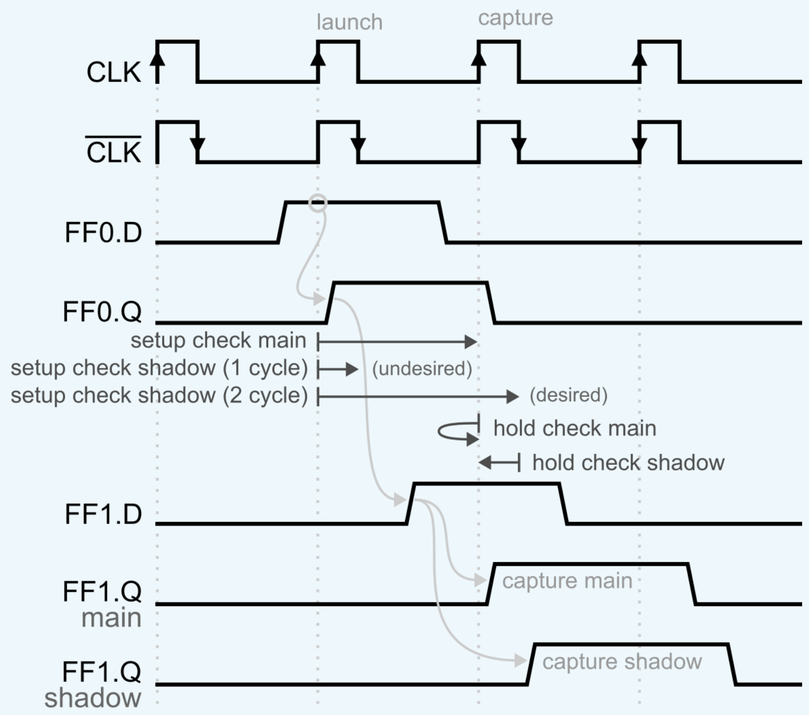
- 1271 MeV Xe ion source with LET 62.5 MeV cm²/mg shows 5% of the SEUs were not reported.
- Two photon absorption testing shows all SEUs were reported.



DESIGN CONSTRAINTS (SDC) FOR SHADOW FLIP-FLOP

Multi-cycle path timing constraints must be applied to all shadow flip-flops. These constraints assure proper setup and hold requirements.

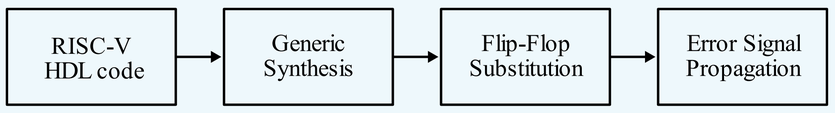
```
create_clock -name clk -period 10ns
    -waveform {0 0.5ns} [get_pin clockGen/out]

set_multicycle_path 2 -to [get_pin *shadow*/Q]
```



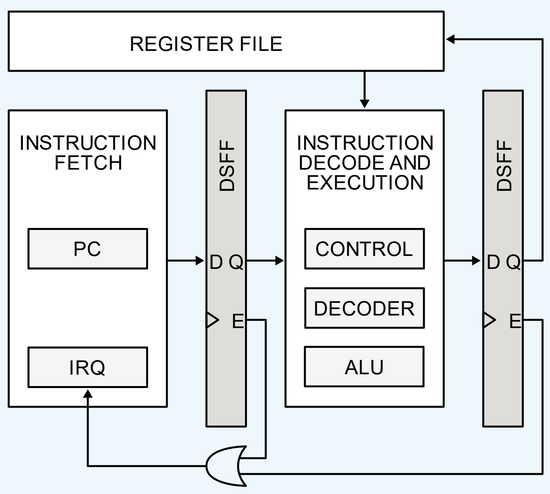
Setup and hold timing with double sampling flip-flops

IMPLEMENTATION IN RISC-V

1. Elaborate or synthesize the design.
2. Substitute flip-flops in the pipeline of processor with DSFFs.
3. Propagate and connect error signals to the interrupt controller (IRQ) with OR-compression.



Implementation of DSFFs in a design



Ibex RISC-V processor wit two-stage pipeline with EDFFs connected to the interrupt controller (IRQ).

The RISC-V processor can periodically perform a checkpoint to store the state of the processor to RAM. The interrupt handle function for SEE errors restores the processor to a known state (roll-back).

CONCLUSION

- Able to detect both SEUs and SETs.
- Fully automated detection method.
- Real-time monitoring capabilities.
- Processor recovery possible with roll-back.