## RISC-V Core for Space Microcontroller Applications in Airbus Crisa

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Open-hardware is revolutionizing hardware development, in a manner similar to how open-source software transformed the software industry. It encourages reuse and is being adopted by industry leaders, institutions, and academia alike. This widespread adoption has resulted in a robust supporting community and an increasing pool of open-source development tools.

The open ISA standard SPARC has been the foundation of computing in the European space industry for the past 25 years. However, in the last decade, the open-source ISA standard RISC-V has emerged as a more modern alternative and is rapidly gaining momentum among industry leaders, academia, and institutions.

RISC-V technology offers several key advantages, including no licensing costs, vendor independence, modular architecture, flexibility, and efficiency. RISC-V developers have the freedom to implement their own RISC-V core and tailor the architecture to their specific needs. A large and growing community, an extensive pool of implementations, and development tools are already available to support this.

During the presentation, it will be shown how Airbus Crisa has developed a RISC-V processor core to target embedded microcontroller applications for space, taking full advantage of the modularity, flexibility, and efficiency offered by RISC-V technology. Some key topics that will be addressed include:

- The design process for the core and how it has been hardened against single-event upsets (SEUs)
- The use of open-source tools, libraries, and methodologies to verify and validate the RISC-V core in compliance with Airbus Crisa's ECSS-approved flow.
- The integration of the software development environment and processor debugging capabilities into the core architecture from the outset, to create a comprehensive hardware-software solution.
- The integration of RISC-V in two of our projects, and how it addresses the new challenges and technical requirements of our customers.