# MemoryBoost: RISC-V Temporal Isolation Through Dynamic Hypervisor-level Bandwidth Reservation

Afonso Oliveira[1], Diogo Costa[1], Sandro Pinto[1]

[1]Centro ALGORITMI / LASI, Universidade do Minho, Portugal

**Abstract**

*We introduce MemoryBoost, an open-source, hypervisor-level dynamic Memory Bandwidth Reservation (MBR) mechanism for Mixed-Criticality Systems (MCSs). MemoryBoost leverages deterministic Machine Learning and a VM-centric design for temporal isolation, maintaining OS/platform independence atop the Bao hypervisor with full RISC-V support. Preliminary results show that MemoryBoost reduces performance degradation in critical workloads by up to 70% while maintaining 80% throughput for non-critical workloads, achieving overhead as low as 1%.*

## Motivation

Space missions impose strict constraints on computing platforms, requiring a balance between complex workloads, reliability, and stringent Size, Weight, Power, and Cost (SWaP-C) considerations [1]. This has driven the adoption of Mixed-Criticality Systems (MCSs), consolidating applications with varying criticalities on shared hardware. Paired with the increasing adoption of RISC-V in space, such as ESA's NOEL-V processor, there is a growing need for mechanisms that efficiently achieve temporal isolation in RISC-V platforms [2][3]. Ensuring temporal isolation in these systems is challenging due to contention for resources like (i)memory, (ii)caches, and (iii)the system bus [1]. To mitigate interference, techniques such as cache coloring and Memory Bandwidth Reservation (MBR) have been proposed; however, most existing MBR solutions are coupled to specific operating systems (OSes) or hardware resources [1], limiting their portability and effectiveness across diverse commercial-off-the-shelf (COTS) systems.

## MemoryBoost Approach

We introduce MemoryBoost, a hypervisor-level, dynamic Memory Bandwidth Reservation (MBR) tailored for RISC-V MCSs in space applications. MemoryBoost uses a deterministic Machine Learning (ML) approach to dynamically reserve memory bandwidth to virtual machines (VMs), thereby ensuring temporal isolation. Implemented atop the RISC-V-compatible Bao hypervisor, MemoryBoost requires only a standard Performance Monitoring Unit and a timer. Figure 1 provides a system overview highlighting key innovations:

**1. Non-blocking concurrency Model.** Non-blocking concurrency model that operates on a best-effort basis, ensuring data is never delayed by more than one period. Minimizes overhead and allows for shorter periods.

**2. Event Processing.** Modulo hashing with upper and lower bounds, verifying that input parameters don't cause system errors.

**3. ML model.** A flattened Decision Tree (DT) to dynamically assign MBR budgets. Ensures full determinism and predictability, while creating minimal overhead, with a time complexity O(1) and a minimal amount of branches.

**4. Criticality Assigner.** VM-centric design, where each VM is assigned a criticality level—Catastrophic, Critical, Major, or Minor, following ECSS standards— that directly impacts the budget it is assigned, allowing precise resource allocation based on workload importance.

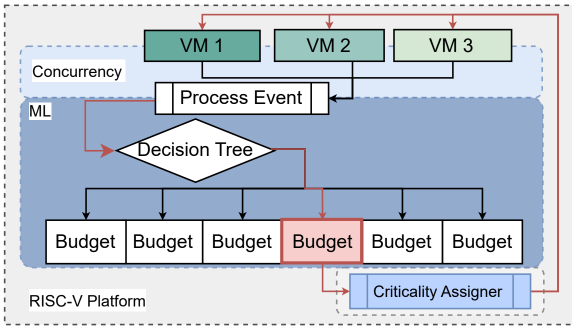


**Figure 1:** *MemoryBoost Overview on a RISC-V Platform*

By combining deterministic ML-driven dynamic adjustments, a VM-centric reservation approach, and a novel concurrency model with low overhead, MemoryBoost stands apart from existing solutions and provides a reliable mechanism for enhancing temporal isolation, predictability, and adaptability in MCSs.

## Experimental Results

We evaluate our mechanism using a setup that runs the MiBench automotive suite alongside a baremetal application invalidating cache lines. With a 100µs period, MemoryBoost improves critical VM performance by up to 70% while maintaining 80% throughput for less-critical VMs, incurring just 1% overhead. Although our results are not evaluated on a RISC-V board, the issue stems from microarchitectural constraints, making it reasonable to expect similar outcomes on RISC-V.

## Discussion & Conclusion

Future work includes testing more platforms and benchmarks as well as evaluating MemoryBoost alongside other mitigation techniques (e.g. cache coloring). MemoryBoost stands as an innovative advancement in temporal isolation, paving the way for space-capable MCSs on RISC-V.

## References

[1] J. Martins and S. Pinto. "Shedding Light on Static Partitioning Hypervisors for Arm-based Mixed-Criticality Systems". In: *Proc. IEEE RTAS*. 2023.

[2] B. Sá, J. Martins, and S. Pinto. "A First Look at RISC-V Virtualization From an Embedded Systems Perspective, 2022". In: *IEEE Transactions on Computers*. 2022.

[3] R. Weigand. *RISC-V: a Rising Star in Space*. 2023.