Flexible and secure payload integration; CDPU a RISC-V 'New Space' approach

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***Abstract*— We have started the development of a new payload Control & Data Processing Unit (CDPU), an Instrument Control Unit (ICU) with additional data processing capabilities targeted towards 'New Space'CubeSat and SmallSat instruments. We defined a modular architecture to allow flexibility in interfaces and functions, with advanced and reliable in-orbit FPGA reprogrammability. The FPGA firmware includes a RISC-V softcore and optional accelerators, allowing for edge processing. The RISC-V System-on-Chip architecture is being improved for reliability with FDIR architectural features, like lock-step and RERI.**

Keywords—ICU, FPGA, SmallSat, RISC-V

I. Introduction

Globally, there is a trend towards the advancement of more versatile onboard hardware platforms, particularly for the upcoming New Space SmallSat constellation segment. Nevertheless, the evolving geopolitical landscape has intensified the call for greater autonomy within the European space sector. Nowadays, there is a need for European non-dependence technology.

Technolution has started the development of a new payload Control & Data Processing Unit (CDPU), an Instrument Control Unit (ICU) with additional data processing capabilities targeted towards SmallSats. The CDPU acts as a hub for (optical) instruments that forms a logical bridge between the instruments and the SmallSat platform. The CDPU allows for easy and quick payload integration in SmallSat platform. It offers standardized hardware interfaces for integrated (optical) instruments, as well as sophisticated facilities for processing the science data before it is sent down to earth. We defined a modular architecture to allow flexibility in interfaces and functions, with advanced and reliable in-orbit FPGA reprogrammability. The component quality class and applied development processes are chosen to target for an in-orbit design lifetime of 5 to 10 years. A standardized modular electronics approach will give instrument developers means for quick instrument development and faster instrument validation cycles. In addition with easy and quick payload integration, the CDPU development will result in quicker time-to-orbit of advanced EO instruments for SmallSats.

The CDPU will become the bridge between the instrument's front-end and the SmallSat platform. Hence, the CDPU hosts the ICU-functionality in the instruments targeted for the SmallSat market. The CDPU is a space avionics unit to control compact (optical) instruments and to process the instrument science data . Under control, we currently assume functions like the provision of switched and conditioned power, the provisions of fine thermal management functions, driving calibration provisions and operational tasks as the management and execution of measurement schedules. Data processing capabilities currently require simple data processing tasks as the binning of pixels, co-adding of science images and packetization of raw data to a proper format for the downlink of the satellite. But, the CDPU will be able to offer more. As instruments are becoming more sophisticated and since there is an increasing demand for in-orbit data processing functions such as compression, data filtering and encryption, the CDPU will contain powerful data processing capabilities like artificial intelligence (AI) methods.

II. MODULAR ON-BOARD ELECTRONICS

The CDPU high-level architecture is a modular electronics concept, illustrated by Fig. 1. The proposed CDPU offers a combination of instrument control functions, interface flexibility and powerful data processing capabilities. This modular concept enables a cost-efficient solution which is suitable for a variety of payloads and platforms.

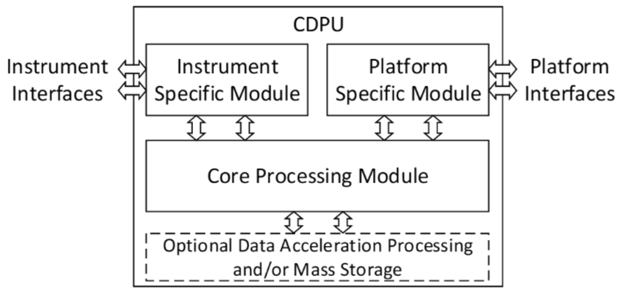

Fig. 1. Modular CDPU architecture.

The *Core Processing Module* is generic for all foreseen CDPUs. It is a single string design and contains high-reliability and high-performance data processing capabilities to support the required data throughput of at least 400 Mbit/s with real-time compressions and/or encryption. Also, the instrument control logic is executed here. TM/TC handling and most instrument control functions are covered by a RISC-V softcore microcontroller. We integrate the FreNox RISC-V microcontroller IP [1] that has its heritage in numerous products for high-assurance and high-reliable security applications for data line encryption and network domain separation (i.e. NLD/EU/NATO-restricted). The applied RISC-V microcontroller supports reliability implementations like lock-step operation.

The *Instrument Specific Module* introduces flexibility of the CDPU to interface with a variety of instruments. Interfaces may be data as well as discrete interfaces. SpaceWire and SpaceFibre interfaces are considered as standard instrument data interfaces. But since the instrument specific module will be tailored made, it can offer full interface compatibility with the optical instrument or other user needs.

The *Platform Specific Module* introduces flexibility of the CDPU to interface with a variety of platforms. It accommodates the high-power functions such as isolated secondary power conditioning and heater drivers. An important function of the platform specific module is failure isolation between payload and platform. This makes the CDPU suitable to fly payloads on satellite missions of all classes.

III. Versatile Design Considerations

Flexibility and versatility are hallmarks of the CDPU's technology. The computational core of the system consists of a radiation-resistant reprogrammable FPGA. Thanks to the FPGA technology it is relatively simple to implement different data processing functionality or to adjust the operational functions. This can even be done after the satellite with the CDPU has been launched and is operational.

The CDPU concept has been defined for design-time and run-time flexibility based on the following considerations:

- A larger independence from the platform also means that the CDPU takes over more instrument-related operational functions from the platform. This means that the CDPU allows for more instrument autonomy by execution of mission timelines and handling of FDIR (Failure Discovery, Isolation and Recovery) at the CDPU without platform interaction.
- Important on-board data processing features that are considered to be at least supported are: *science data encryption*, *real-time data compression and filtering* in order to optimise the data product value of a mission, and for the mid-term future *Artificial Intelligence (AI)* features for tip and cue type missions are foreseen, which need additional processing power.
- Instrument developers want to be as flexible as possible in terms of interfaces to enlarge their marked potential. The CDPU allows to accommodate payloads on single payload MicroSats (one-offs or constellations) as well as hosted payload on bigger platforms. Thanks to the modular architecture, the CDPU enables an instrument to be accommodated on multiple platforms with minimum platform interface engineering effort.
- Instrument developers are interested in a CDPU with basic functional software implemented. On top, instrument developers want to develop the application software by themselves to reduce supplier interaction and development time. Software flexibility, by leveraging the RISC-V ecosystem, allows a shorter time to orbit for the instrument developers.

IV. Reconfigurable FPGA with RISC-V softcore

The *Core Processing Module* of the modular CDPU demonstrator is based on the Microchip PolarFire FPGA. This FPGA is selected since it is flash-based, since it is one of the most power-efficient solution for the required functions and since it is available in various quality grades. We have implemented our AXI4-based system-on-chip with RISC-V microcontroller into the PolarFire FPGA, including two SpaceWire (SpW) interfaces for interfacing with the instruments and the platform. SpaceFibre (SpFi) can also be used for higher data throughput. The AXI4-based interconnect also accommodates function accelerators, such as compression and security functions.

FreNox [1] is our implementation of the RISC-V open standard. It was developed entirely in-house for classified security applications, and has no dependencies on open-source implementations. We thus have full control over the design; this offers advantages, for instance during verification, validation or certification of critical safety and security applications. Also, we have implemented and demonstrated the FreNox RISC-V architecture in the European FPGA technology from NanoXplore. Driven by the need for European non-dependence technology, we anticipate the development of a *Core Processing Module* built on European FPGA techology.

V. Use-case Payload Demonstration

For a successful development and demonstration of the CDPU, early adopters have been involved from the start of the CDPU specification phase. With the support from our partners, we have built a demonstrator integrating a SPEXone instrument [2][3] together with the CDPU. Fig. 2 shows the data handling architecture that is used during this real-life demonstration showcase.

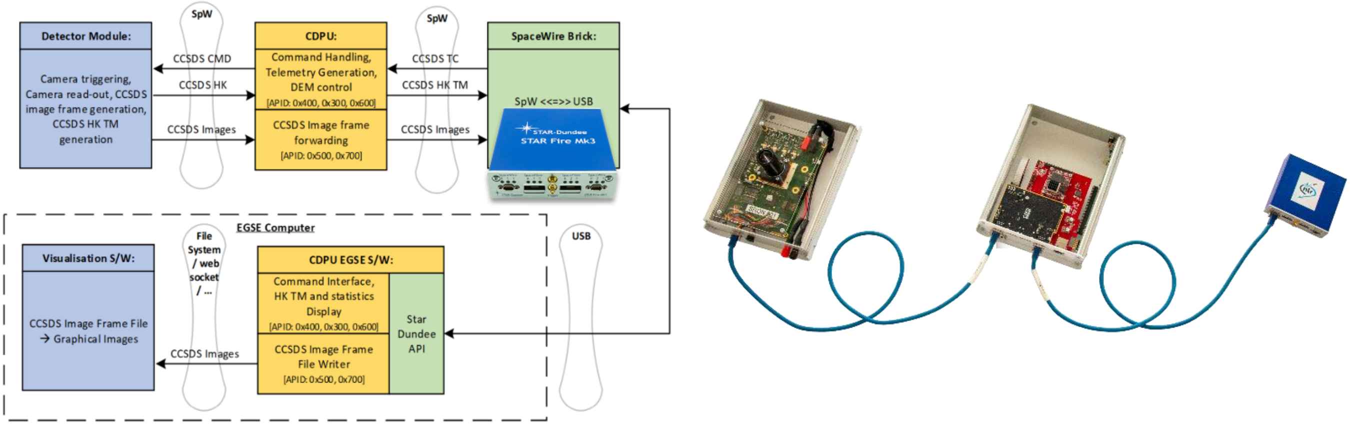

Fig. 2. Data handing architecture of the lab model demonstration.

VI. CDPU State-of-Art

The presented CDPU is a novel RISC-V powered payload control and data processing unit that is able to serve the evolving SmallSat market and is a perfect-fit solution for compact instrument developers. Besides the technical advantages, it provides a good separation of concerns between instrument developers and platform provider allowing short time-to-orbit of payloads and missions. The CDPU design is prepared to enable missions profiting from current and near future space developments as advanced on-board data processing techniques and hardware, advanced and high data volume payload concepts and low latency in-orbit data networks.

A lab model of the CDPU has been developed and successfully demonstrated with the SPEXone instrument front-end. At the moment the Flight Model development phase is being started, and plans are prepared to adopt to the Advanced Data Handling Architecture (ADHA).

To make sure that the system functions correctly and that the data and results are reliable, Fault Detection, Isolation and Recovery (FDIR) schemes will be implemented. This requires the system to detect and if possible correct errors in real-time. For the system to be able to correctly identify and handle errors, the standardization efforts of the RERI (RAS Error-record Register Interface) RISC-V Working Group are being adopted.

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