Enhancing Cache Coherent Interconnects to support Space Systems

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RISC-V IN SPACE

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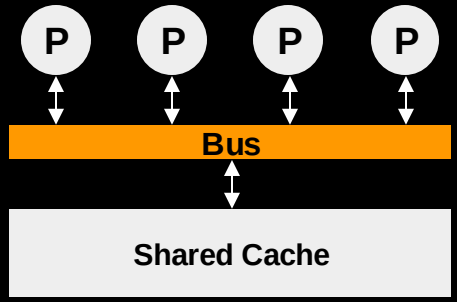
🚀 Rising Computational Demands in Space SoCs

- Key trends:
  - Increased onboard autonomy and AI workloads
  - Higher sensor data throughput
  - Growing application diversity
  - Increased adoption of RISC-V

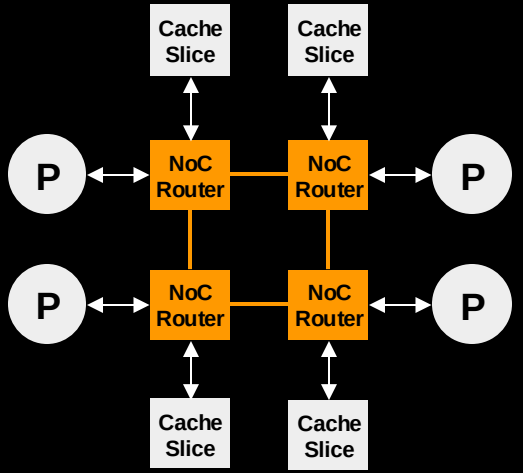
- Architectural Response:
  - Multi-core & heterogeneous processing
  - Dedicated accelerators
  - Complex memory hierarchies and interconnects

System Design Complexity - Interconnect

- Bus
  - Blocking: one transaction at a time
  - Limited Scalability
  - Simple control logic



- NoC
  - Packet-switched
  - Non-Blocking: multiple transactions in parallel
  - Highly scalable and modular
  - Higher throughput
  - Complex network router architecture



System Design Complexity - Coherence

- Need for Cache Coherence
  - Shared memory abstraction to simplify programming
  - Essential for data consistency in parallel processing
  - Enables safe, efficient data sharing among CPUs and accelerators

- Some industrial standards

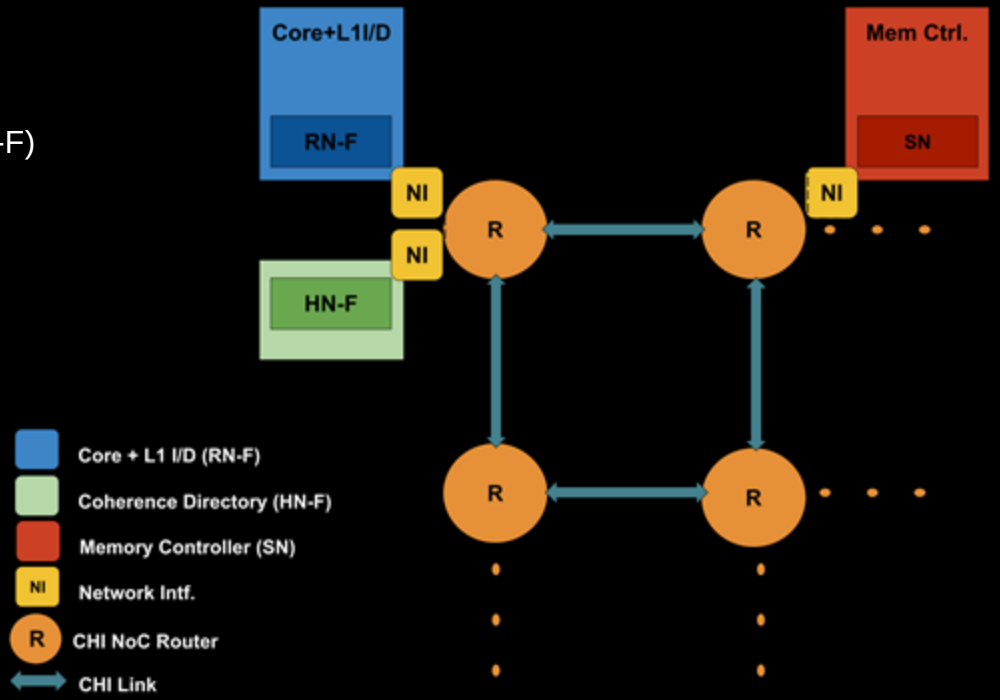
Standard	Developed By	Purpose
AMBA ACE	ARM	AXI coherency extension
AMBA CHI	ARM	Scalable coherent SoCs (core-to-core, IO, clusters)
TileLink	SiFive / CHIPS Alliance	Coherent interconnect for RISC-V SoCs
CXL	Industry Consortium	Coherent CPU-to-accelerator communication over PCIe

IP Development at Chalmers

- IPs:
  - AMBA CHI-Based Coherence Controller
  - FastTrack NoC
- Focus on high-performance systems
- Implemented and tested in various projects (EPI, CSSTII, eProcessor, SGA2, EuPilot)

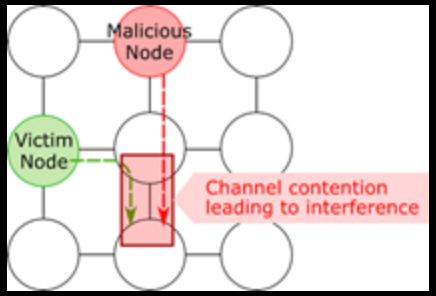
System Architecture

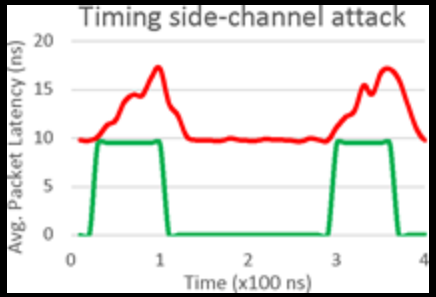
- Coherence Agents (CHI)
  - Fully-Coherent Requester Nodes (RN-F)
    Processor core / cluster
  - Fully-Coherent Home Node (HN-F)
    Shared Cache + Coherence Directory
  - Subordinate Node (SN)
    Memory Controller
- NoC
  - Network Interface (NI)
    Translates messages into packets
  - Routers (R)
    Controls the packet flow
  - Links
    Transfers the packets



Enhancements for Space - NoC

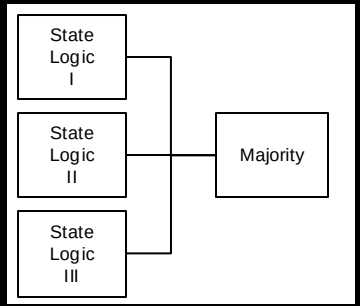
- Lower packet latency using pipeline stage bypassing in the FastTrack NoC
- Traffic isolation → QoS support, Secure communication channels
- Fault tolerant features: error detection/correction, packet retransmission

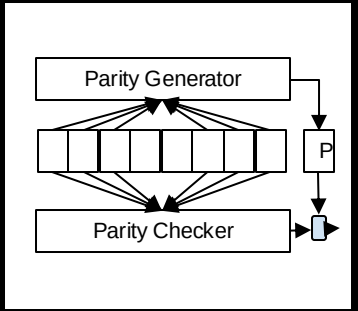




Enhancements for Space - Coherence

- Redundancy for low-overhead logic
- Parity/ECC for presence bits storage
- Protocol-level upgrades to support packet retransmission





Conclusion

- Demands for larger and more complex SoCs in space is increasing
- Scalable NoC based architectures with coherence support are needed
- Security and fault-tolerant features are required for space
- Our team is working on further development of cache coherence and interconnect solutions to bring scalable SoCs into space

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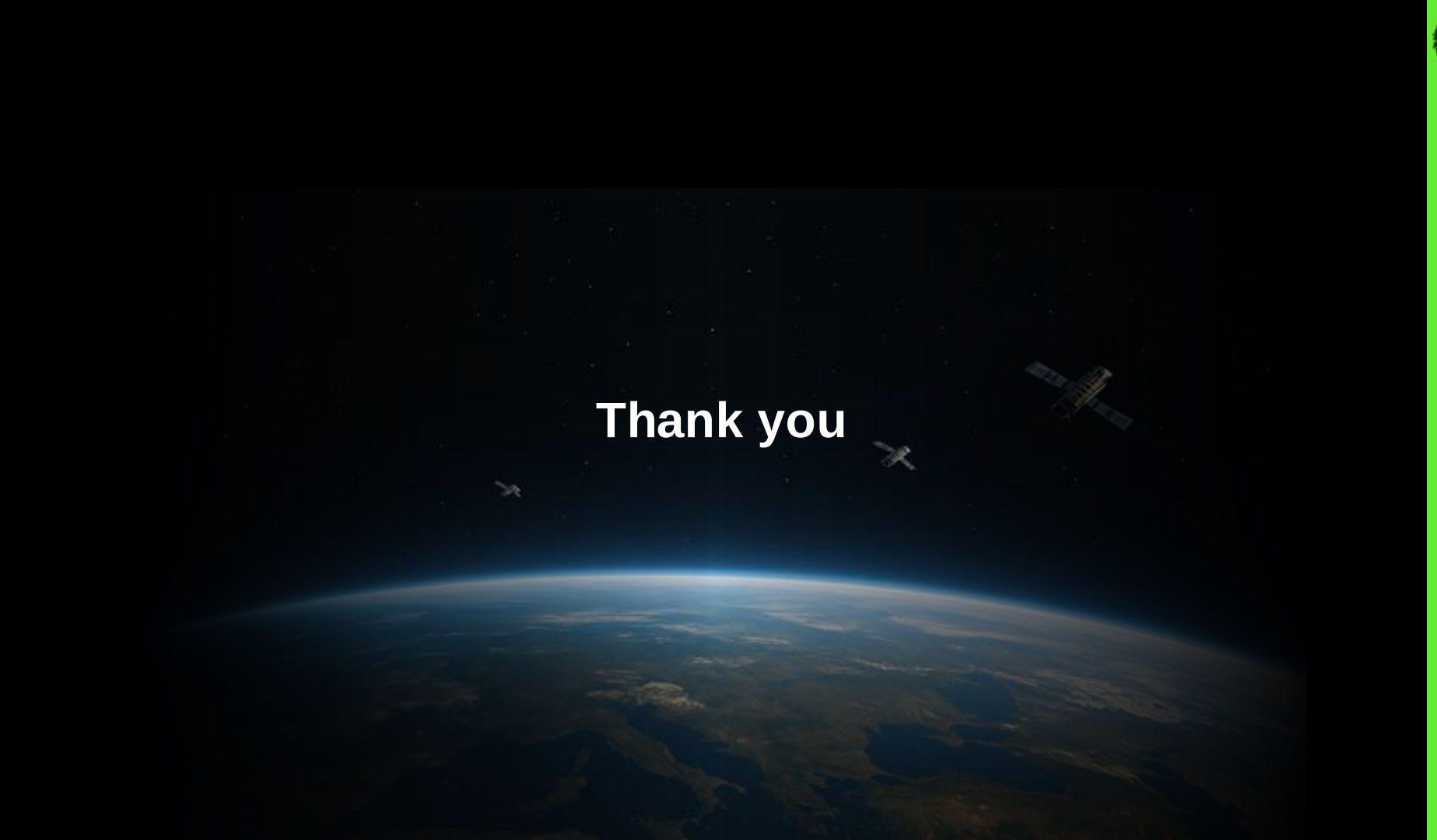
Thank you