Efficacy of Radiation Hardening by Design Techniques on an ASIC 32-bit RISC-V Microcontroller

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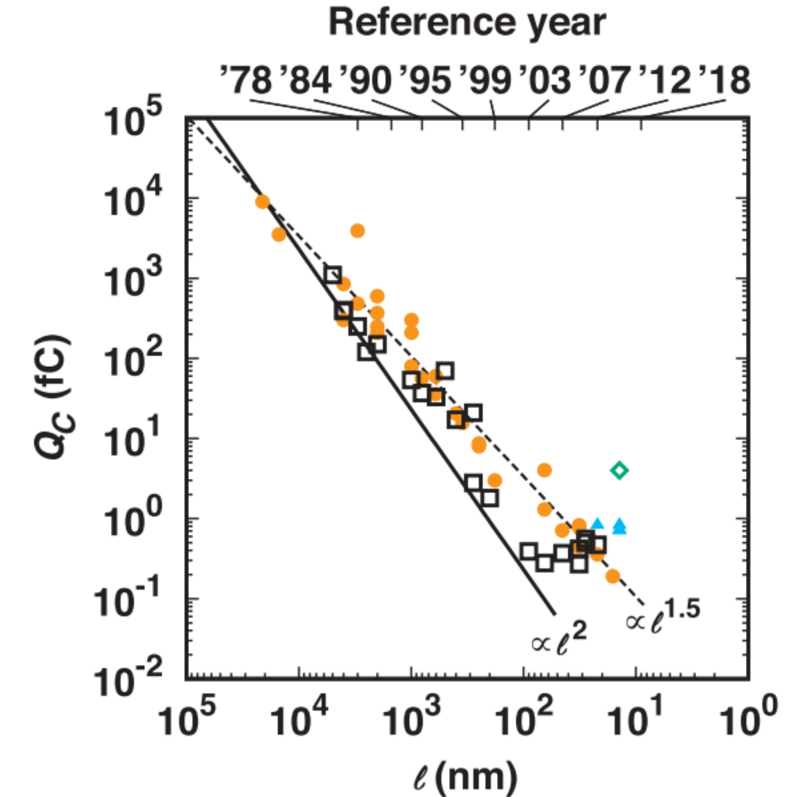
[2]Cisco Systems, CA, USA
[3]QuickLogic Corporation, CA, USA

Presentation to

Motivations

- **The RISC-V ISA has made large strides in the space industry recently**
- **Singe Event Effects (SEEs) continue to be a significant reliability issue**
  - And continue to get worse as technology nodes scale down!
- **More work is needed to understand how best to harden and evaluate devices for high reliability situations**



	Substrate	
Channel	Bulk	SOI†
Planar	Bulk-Planar ●	SOI-Planar □
Fin*	Bulk-Fin ▲	SOI-Fin ◇

† Includes similar substrate structures such as SOS.
* Includes similar three-dimensional channel structures such as a tri-gate.

D. Kobayashi, in IEEE Transactions on Nuclear Science, Feb. 2021,

Presentation Outline

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Semiconductor Technology And
Rad-Effects Research Lab

1. Introduction & Background
2. Device Overview
3. Applied Hardening Techniques
4. Experimental Setups & Results
5. Concluding Remarks

- **In digital systems transient pulses from particles can manifest into a Single Event Upsets (SEUs)**
- **SET → SEU (Bit-Flip)**

1. Introduction & Background

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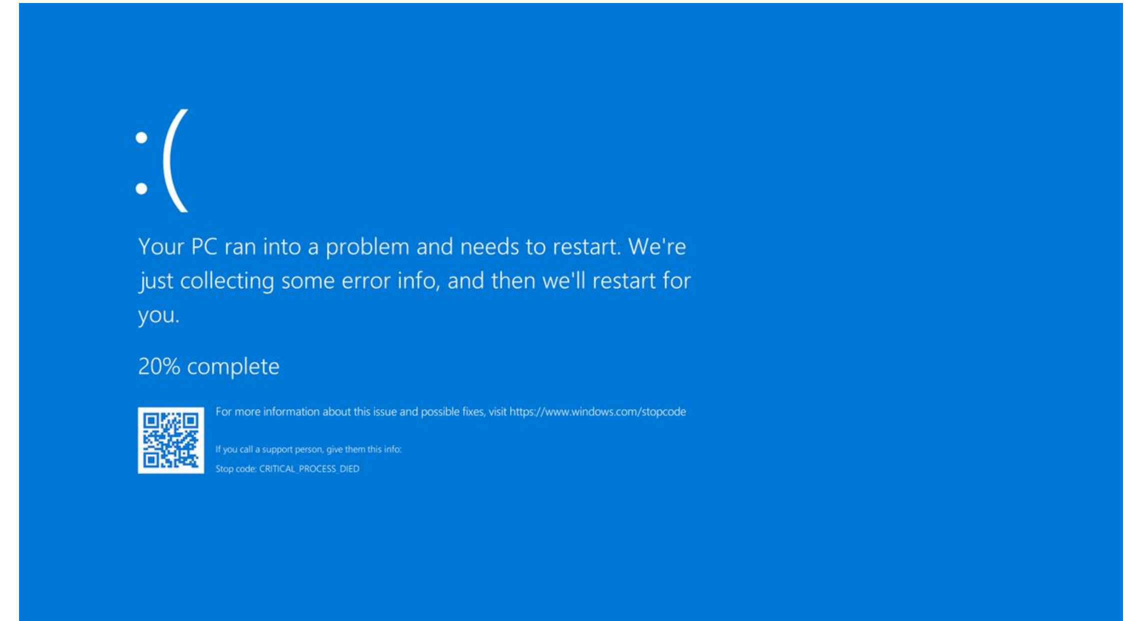
- In digital systems transient pulses from particles can manifest into a Single Event Upsets (SEUs)
- SET → SEU (Bit-Flip)

- **Bit-flips in complex devices, such as microcontrollers, can result in a variety of device failures**

1. Introduction & Background

- **Bit-flips in complex devices, such as microcontrollers, can result in a variety of device failures**
  - Corrupted Data
  - Unintended program jumps
  - Device halts
  - Complete System Crashes
  - Etc



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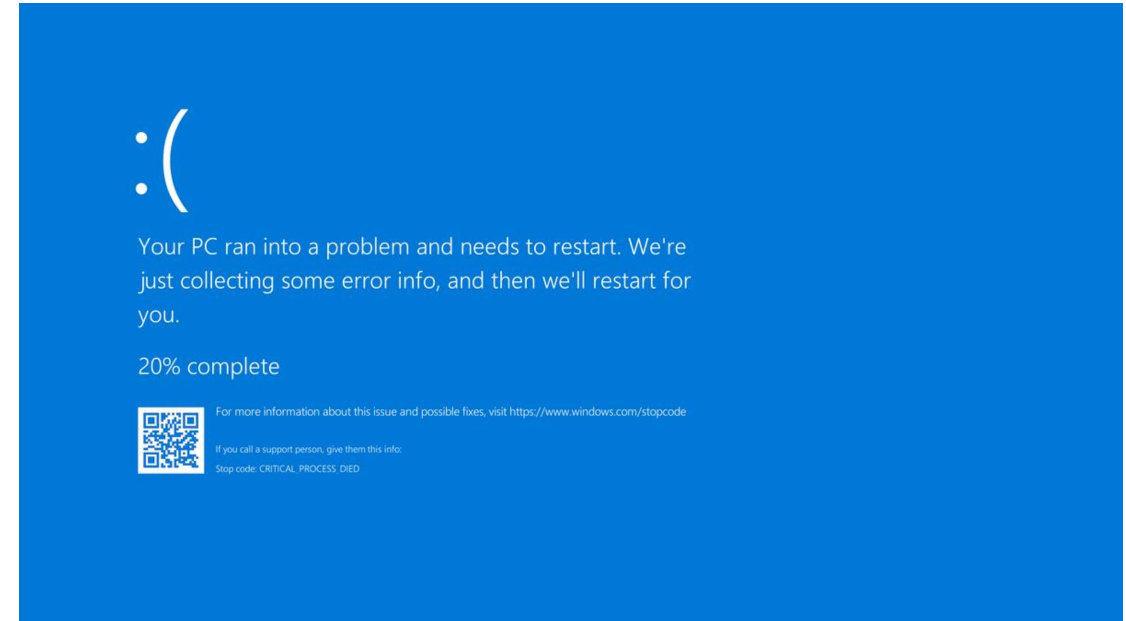

- **For radiation rich environments, like space, companies provide suitable devices to mitigate the possibility of these errors**

1. Introduction & Background

- **Currently there a number of “rad-hardened” devices available**

1. Introduction & Background

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■ Currently there a number of "rad-hardened" devices available

TI TMS570-SEP

- 30 kRad
- SEL > 43 Mev·cm²/mg
- 300 MHz Clock

Vorago VA41630

- 200 kRad
- SEL > 110 Mev·cm²/mg
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Microchip VA41630

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SEU performance data is limited, or not provided – how is the device hardened?

2. Device Overview

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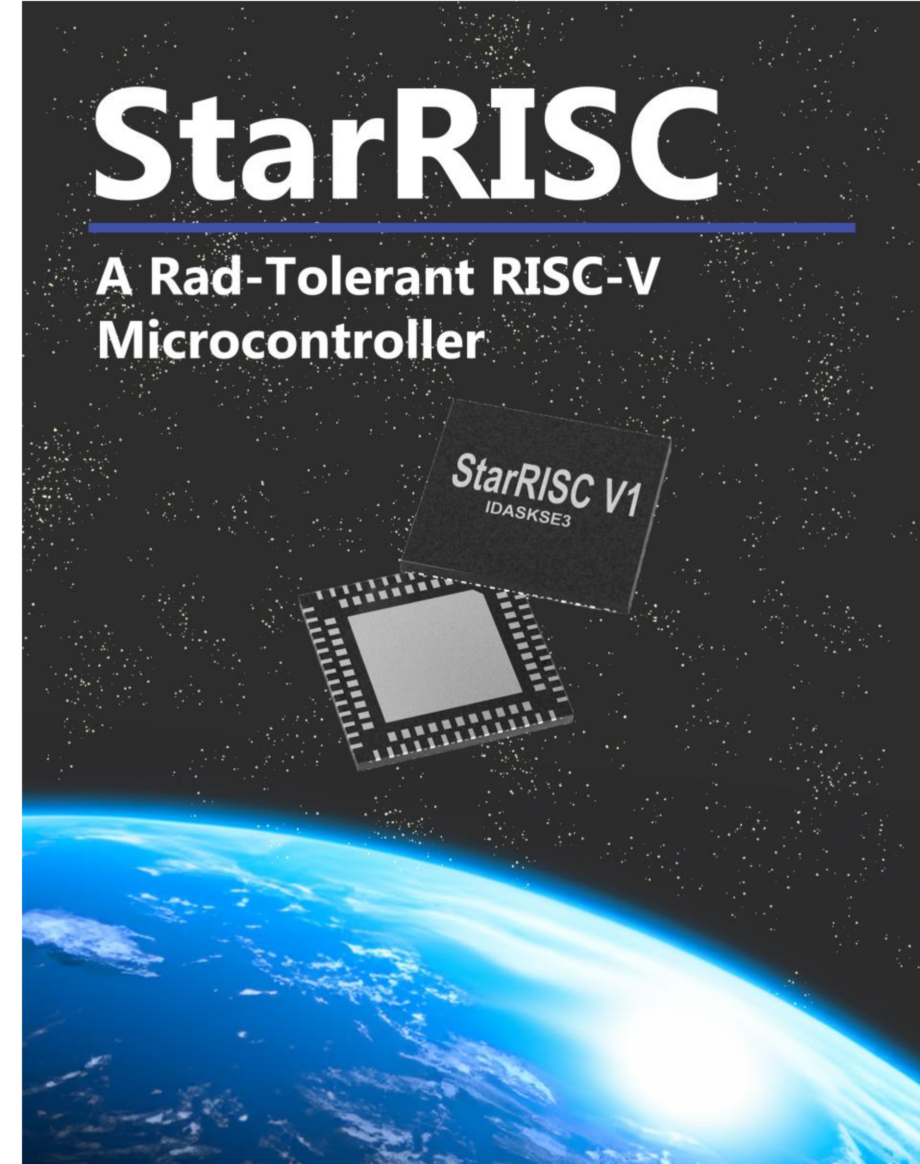
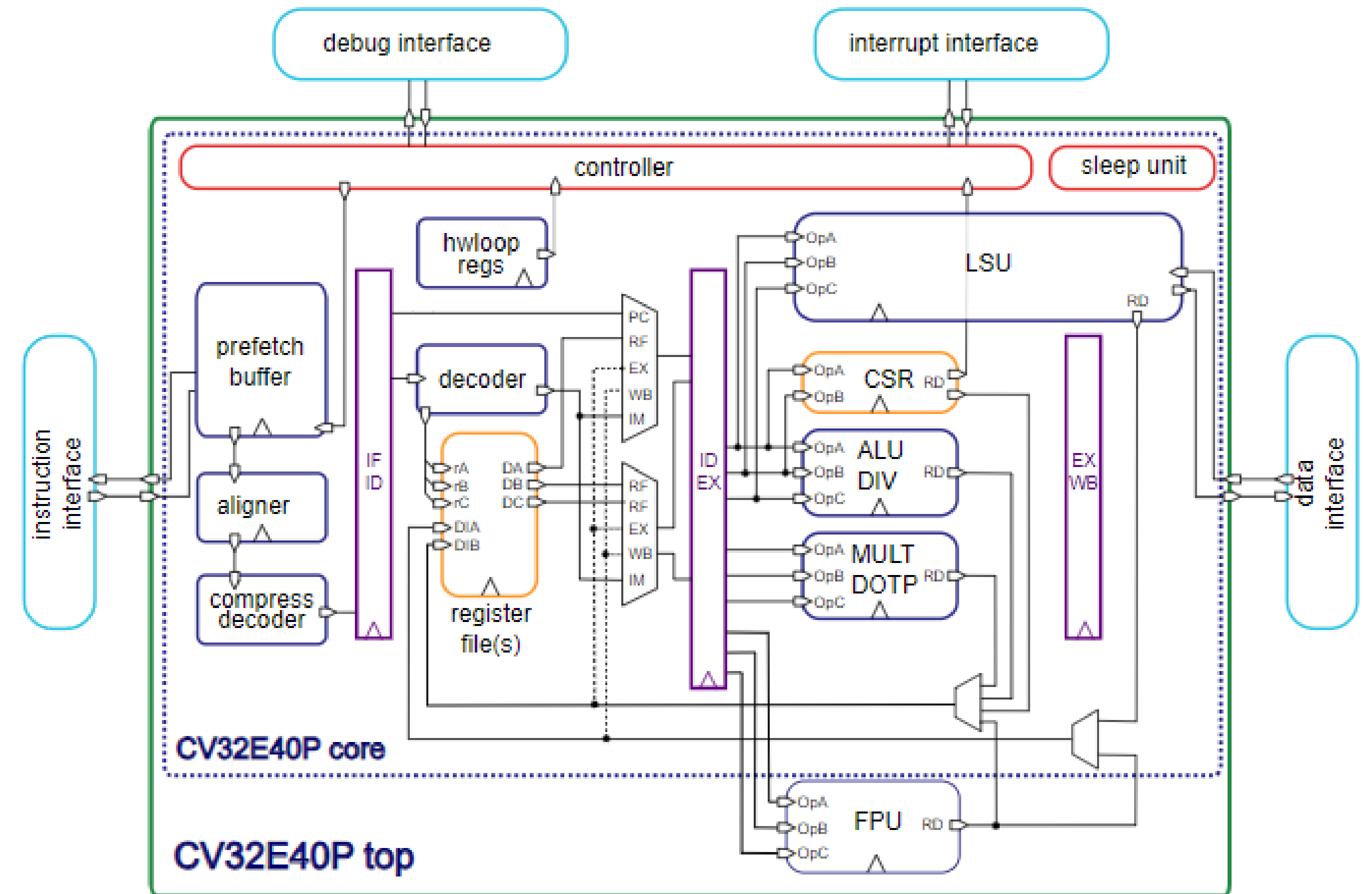
- **StarRISC is radiation-tolerant RISC-V microcontroller device**
  - Built using Global Foundries 22-nm FD SOI technology
- **Utilizes open-source designs, and custom-designed rad-hardened components**
  - Built upon the CORE-V-MCU Project[1]



[1]https://docs.openhwgroup.org/projects/core-v-mcu/doc-src/overview.html

2. Device Overview

- The device features a small and efficient 32-bit core from OpenHW Foundation[2]
- The core is fully open-source, with configurable options

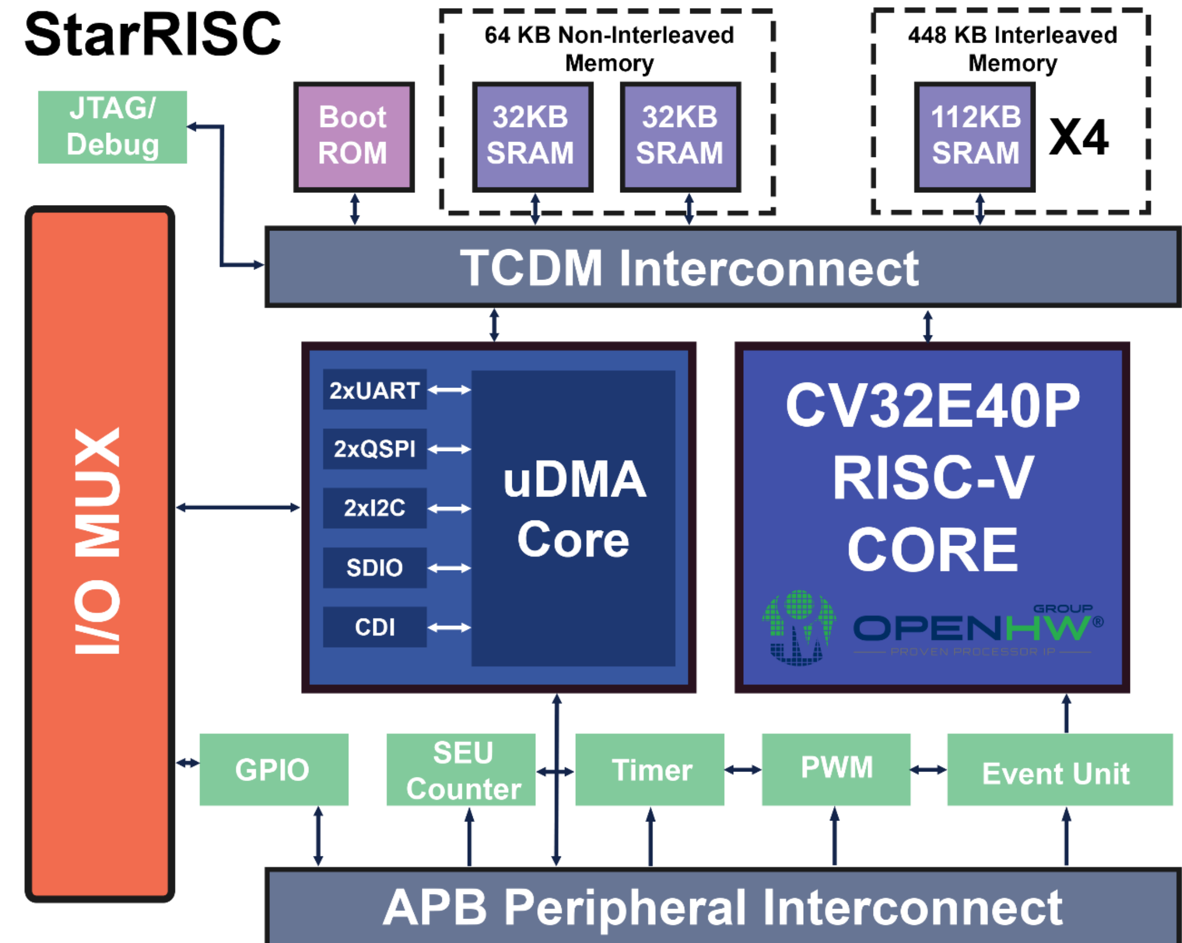


OpenHW CV32E40P Architectural Block Diagram

https://github.com/openhwgroup/cv32e40p

2. Device Overview

- **StarRISC is a full System-On-Chip device**
  - 512 KB of ECC SRAM
  - UART x2, I2C x2, QSPI x2, GPIO x32
  - Internal SEU counters
  - PWM & Timers
  - FreeRTOS Support
  - On-board hardened PLL
    - Up to ~300 MHz



StarRISC Architectural Block Diagram

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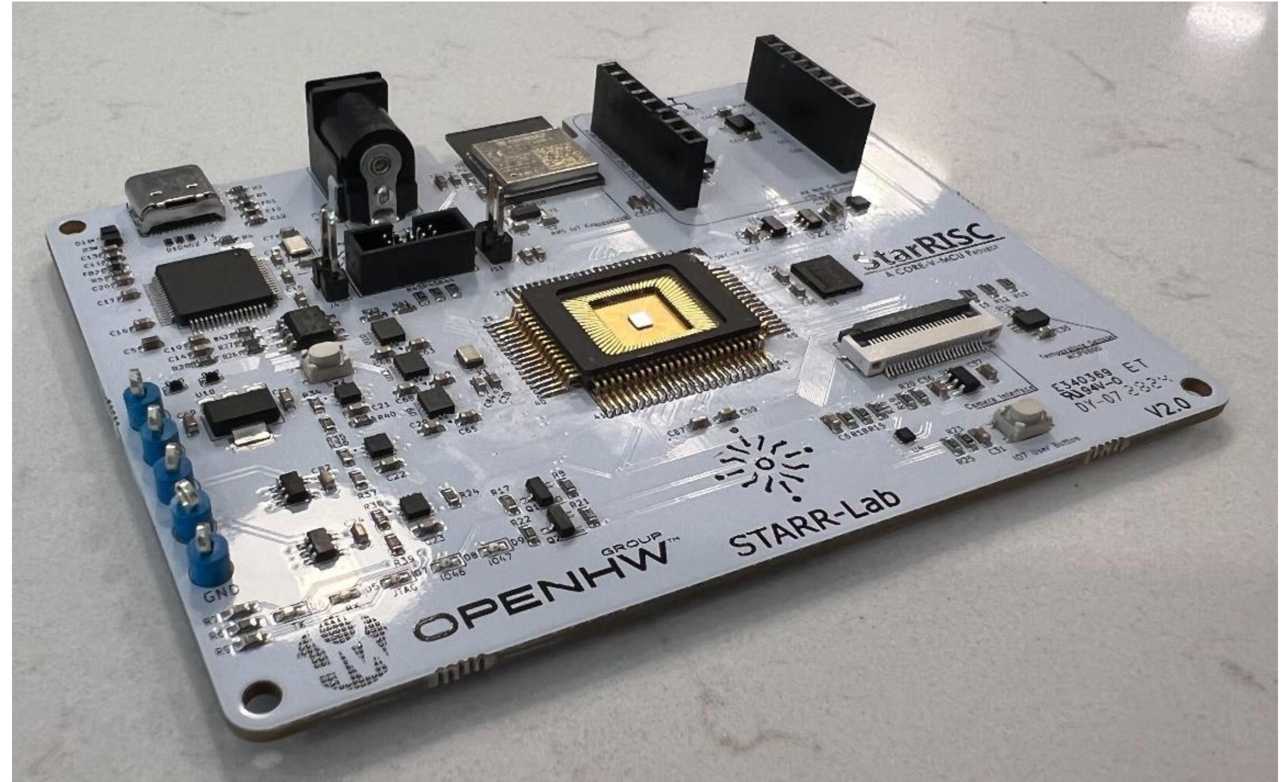
- **StarRISC is supported by a development kit board**
  - Power via USB or 9V
  - Onboard FTDI JTAG
    - And external port
  - Onboard flash memory
  - ESP32 for wireless access
  - & more!



StarRISC Exposed Die & Development Kit Board

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  - ESP32 for wireless access
  - & more!
- **As well as an eclipse-based SDK**
  - GCC support

StarRISC & Core-V-MCU SDK

3. Hardening Techniques

- **StarRISC utilizes a few techniques to reduce its soft error rate (SER):**

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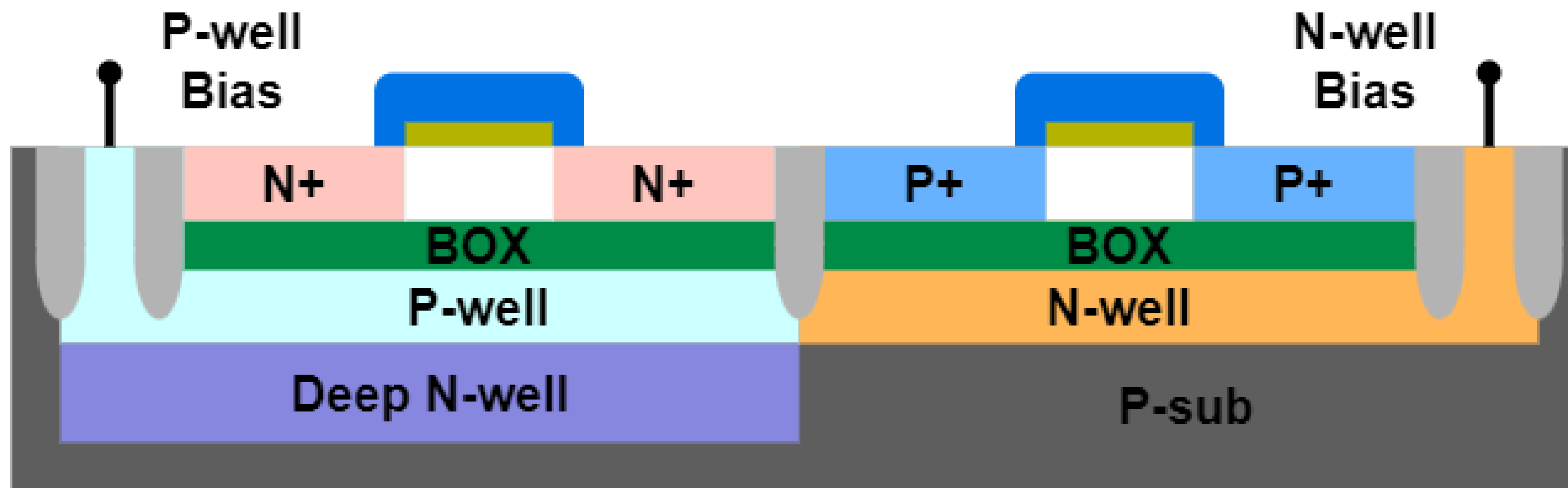

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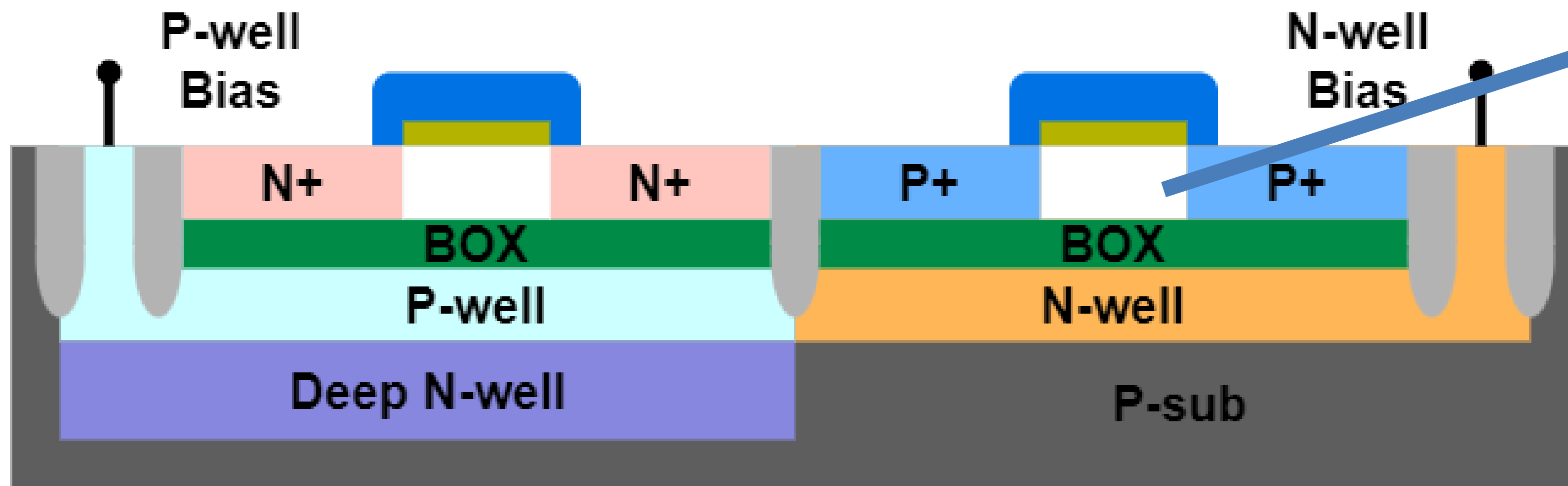

Smaller active area -> less collected charges

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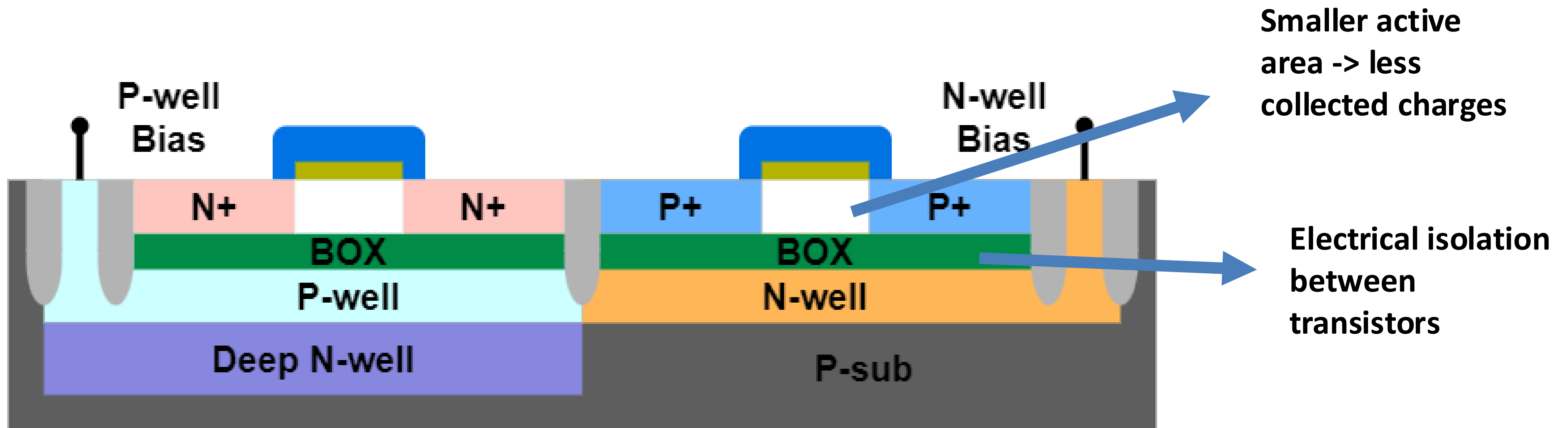

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Electrical isolation between transistors

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   - SECDED scheme used to repair and monitor for errors
   - Alterations to µDMA core to auto-correct upsets on memory reads
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3. Hardening Techniques

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  - All make use of the “Transistor-Stacking” technique

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Standard Latch

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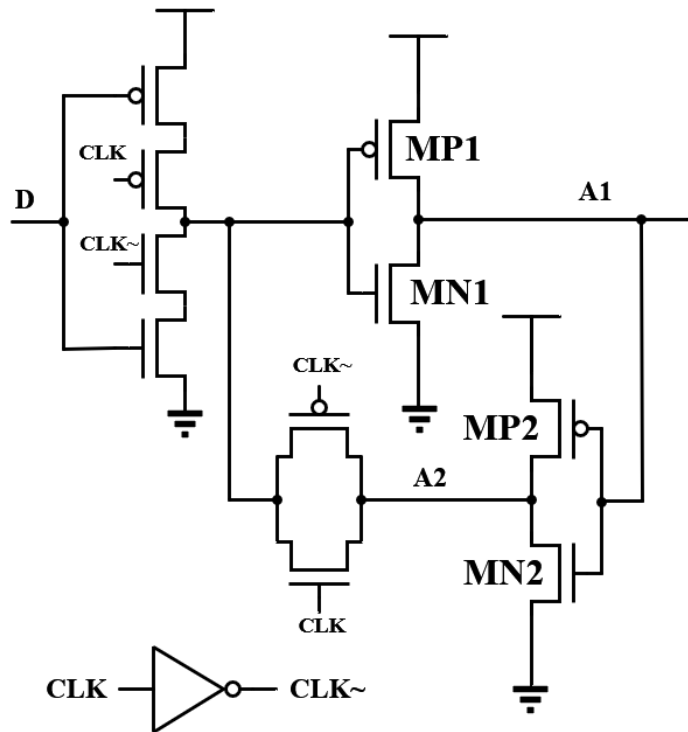

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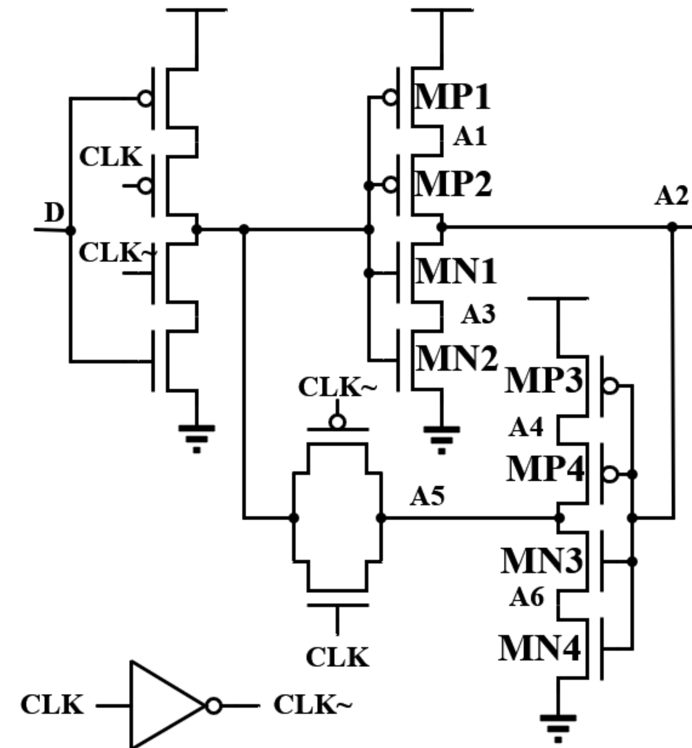

Stacked Transistor Latch

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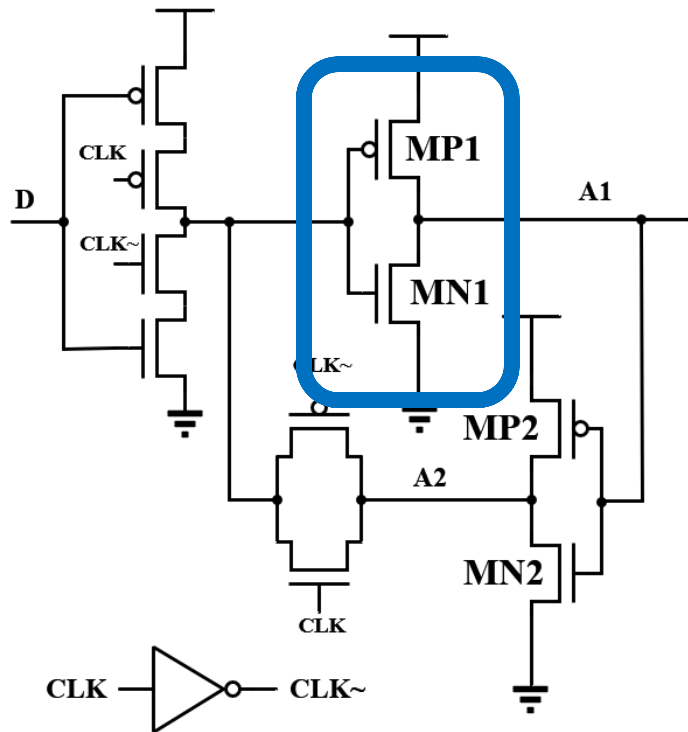

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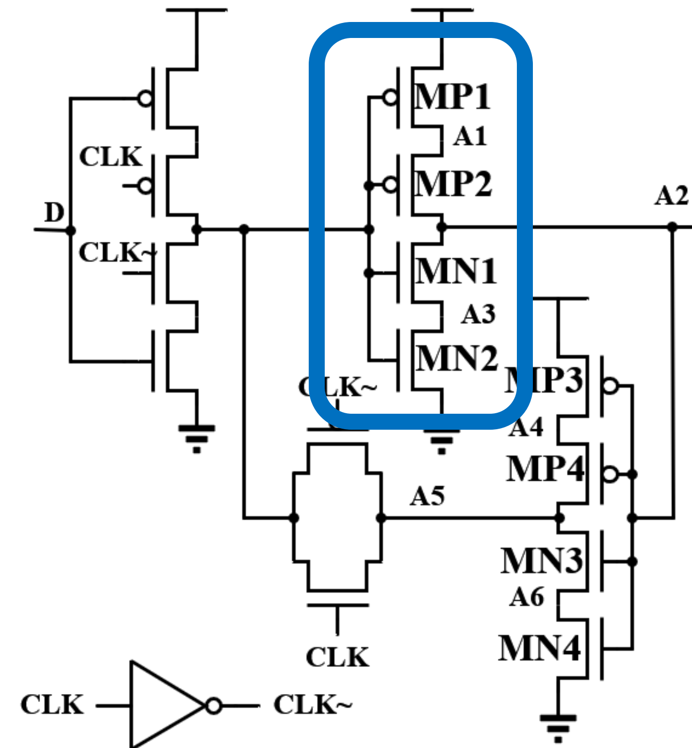

Stacked Transistor Latch

3. Hardening Techniques

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- **At the transistor layout level, we also make changes to the design to induce more complex charge-collections[3]**
  - Which reduce the amplitude of voltage transients

FF Comparison Table

FF Type	Power Usage (n.u)	CLK-Q Delay (n.u)	Cell Area (n.u)	LET Threshold ($Mev{\cdot}cm^2/mg$)
Standard Cell	1	1	1	~1
Hardened Cell	1.4	1.4	1.6	>120

With moderate performance penalties we can obtain extremely hardened cells

Z. Li *et al.*, "Efficacy of Transistor Stacking on Flip-Flop SEU Performance at 22-nm FDSOI Node," in *IEEE Transactions on Nuclear Science*

4. Experimental Setups & Results

- For all irradiation experiments the same test setup was used:

- A test program sends out data logs to be monitored for events
- Extra data about the device can be dumped through the JTAG port and saved via the SDK

4. Experimental Setups & Results

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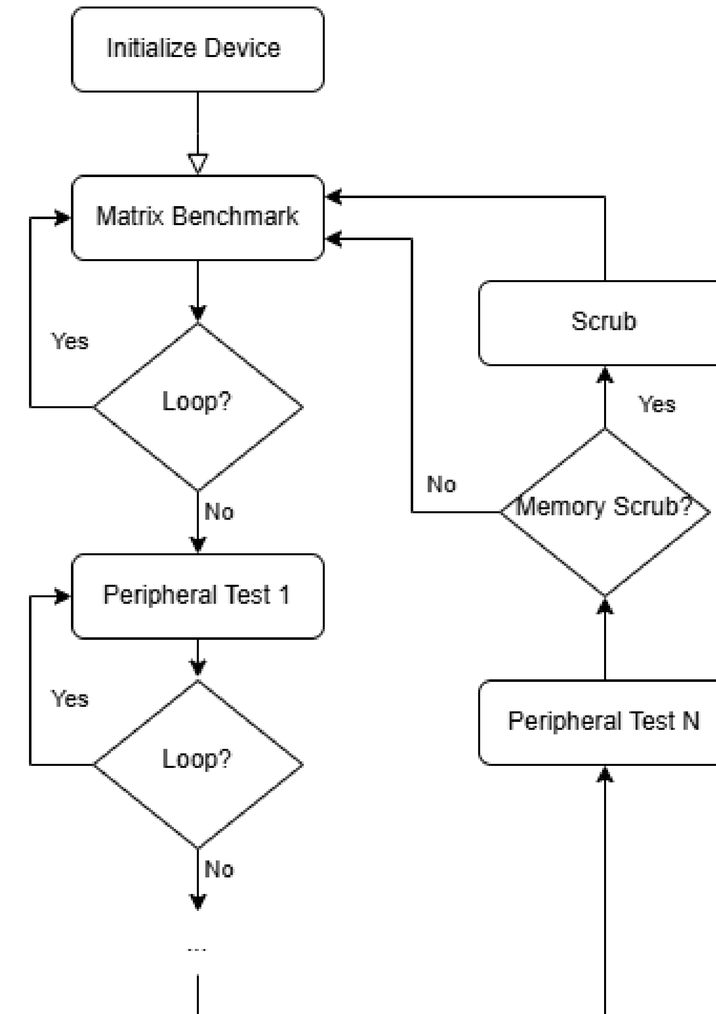
- **The testing software used runs a variety of tests monitoring various functionality of the device**
  - Can be configured between **looped**, and **non-looped** modes
- **SBU and DBU counts are logged after each unit test**



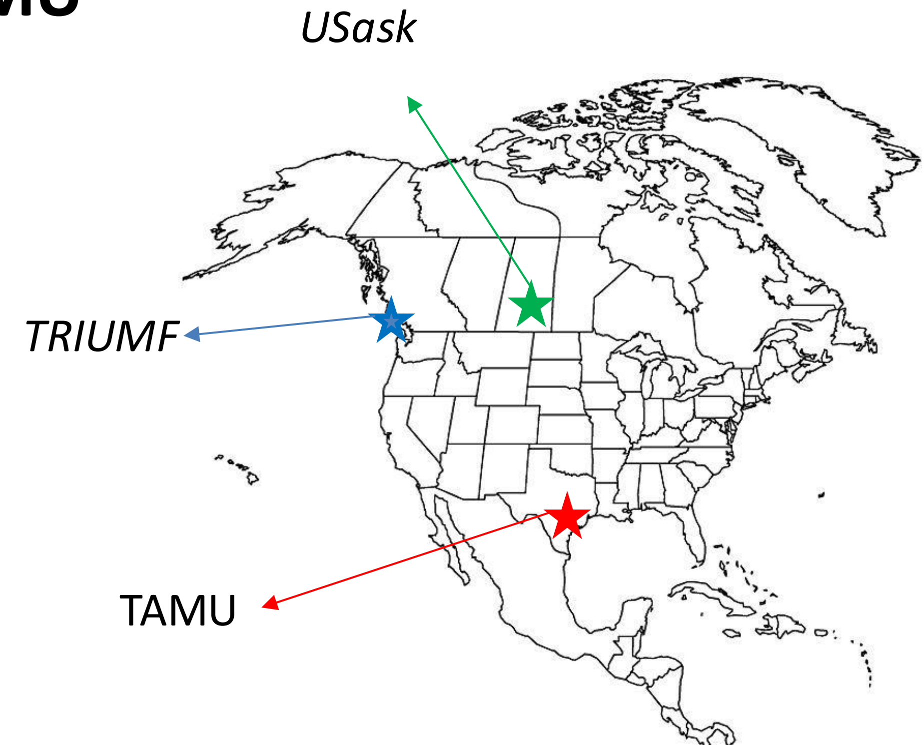
Test Software Flow

4. Experimental Setups & Results

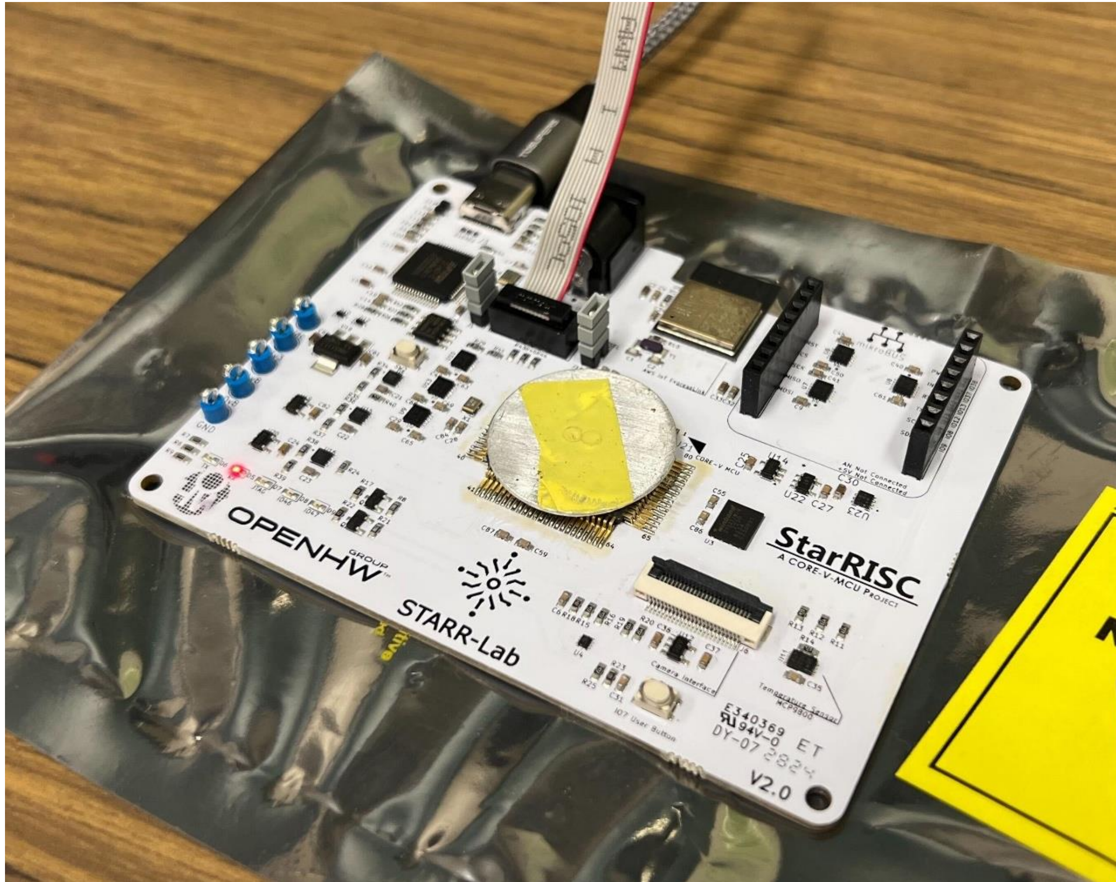
- **Alpha particle irradiation was performed at USask**
- **Proton experiments were conducted at TRIUMF using 150 MeV protons**
- **Heavy Ion experiments were done at TAMU**
  - 1E4 particles/cm^2 flux rate

Ions used @ TAMU

Ion	Linear Energy Transfer (MeV·cm^2/mg)	Range in Si (µm)
Cu	18.4	155
Kr	30.1	149
Ag	43.5	130
Pr	64.1	135



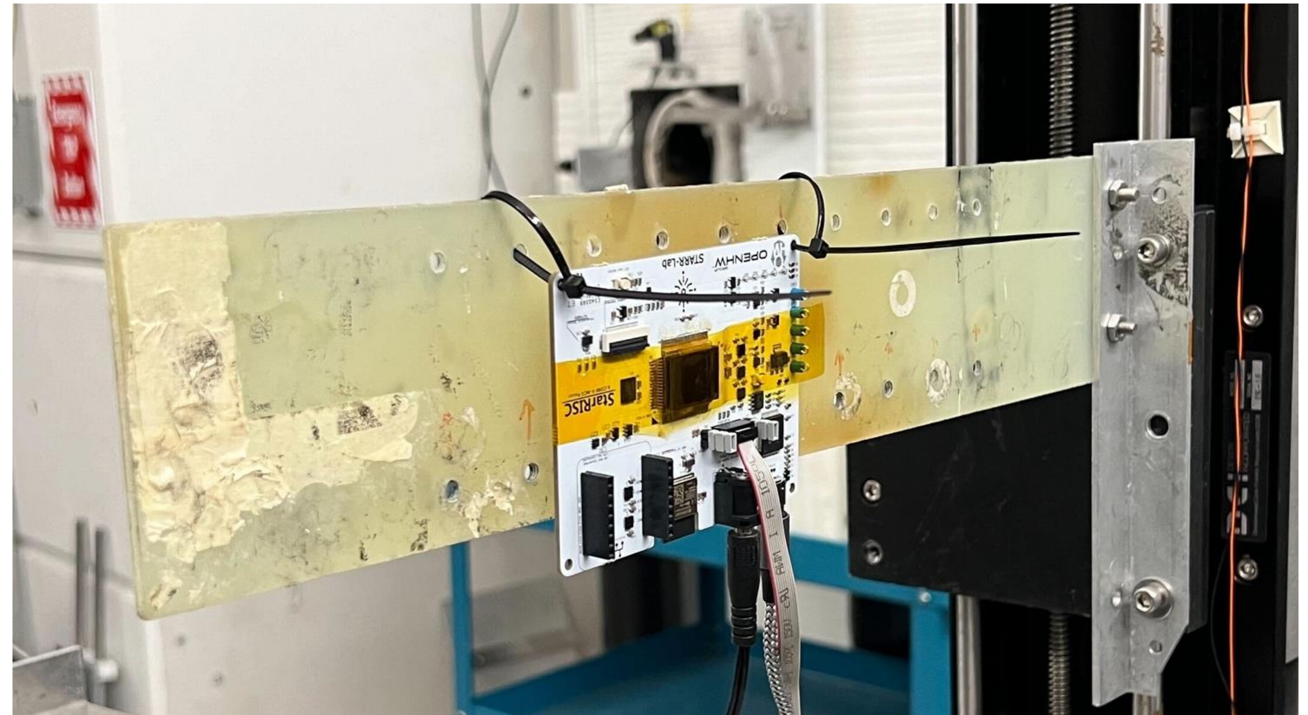
4. Experimental Results – Alpha Particle



- We use an Am-241 source placed directly over the die
- For non-looped testing, no failures or crashed observed
  - 50 SBU/min w/o scrubbing
  - 80 SBU/min w/ entire memory scrubbing
- No DBU observed for non-looped testing
- Some DBUs in unused memory if scrubbed after many hours of irradiation

4. Experimental Results – Protons

- **Device was tested with 105 MeV protons up to a combined fluence of 1E12 particles/cm^2**
- **Average SBU rate of 7/minute – non-looped no scrub**
  - No DBUs
- **No functional failures or crashes for either software mode**
- **No increased current draw or failures up to 200 kRad**



StarRISC undergoing proton testing @ TRIUMF

4. Experimental Results – Heavy Ions

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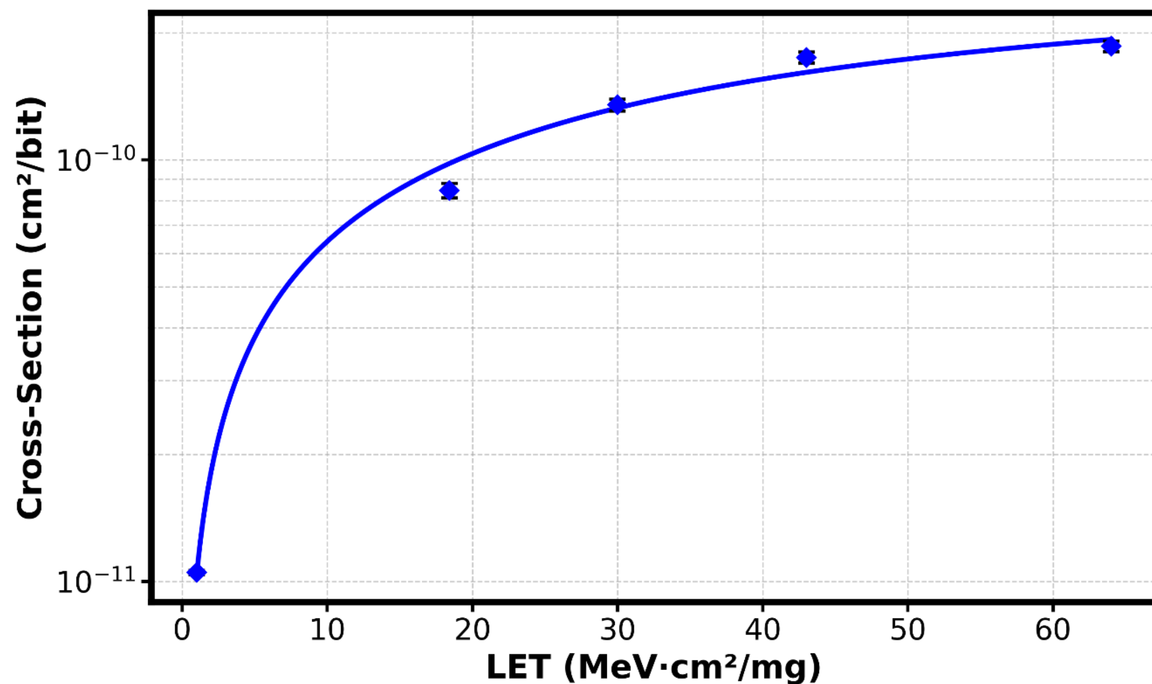
- For ***non-looped*** testing no functional failures or crashes detected up to an LET of 96.3 MeV·cm^2/mg
  - Tested fluence up to 1E7
- ***Looped*** testing presented system failures at every LET tested
- DBUs became much more prevalent

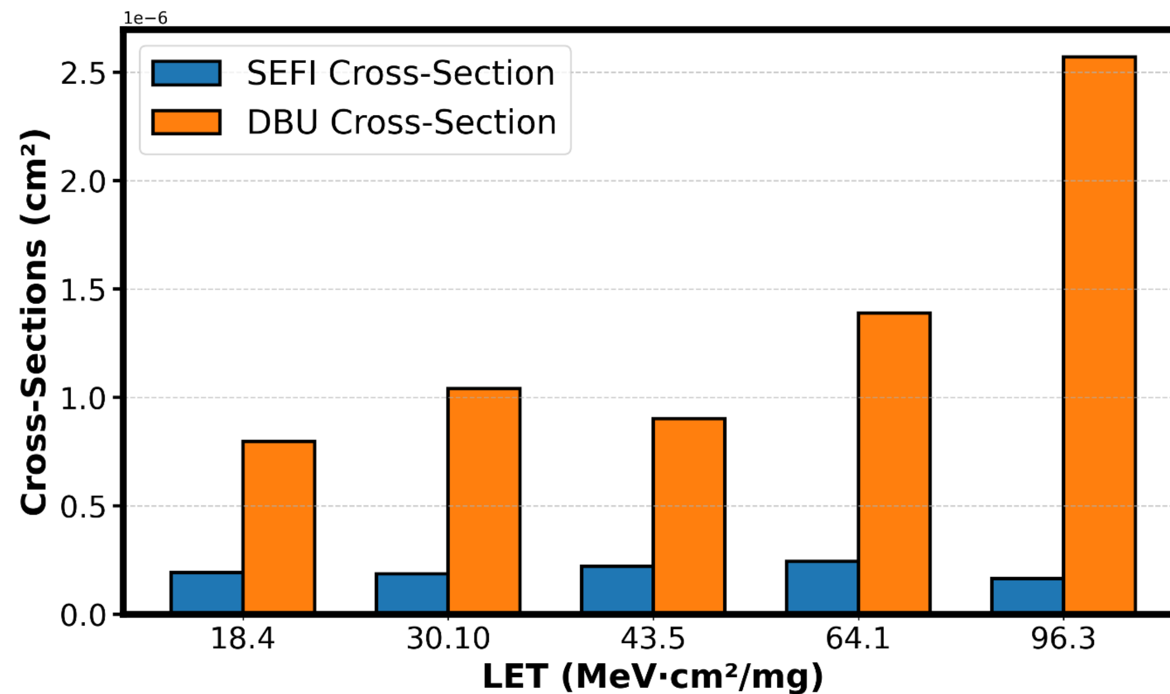
StarRISC undergoing Heavy Ion Testing @ TAMU

4. Experimental Results – Heavy Ions

SRAM SBU Cross-Section Per Bit Vs. LET

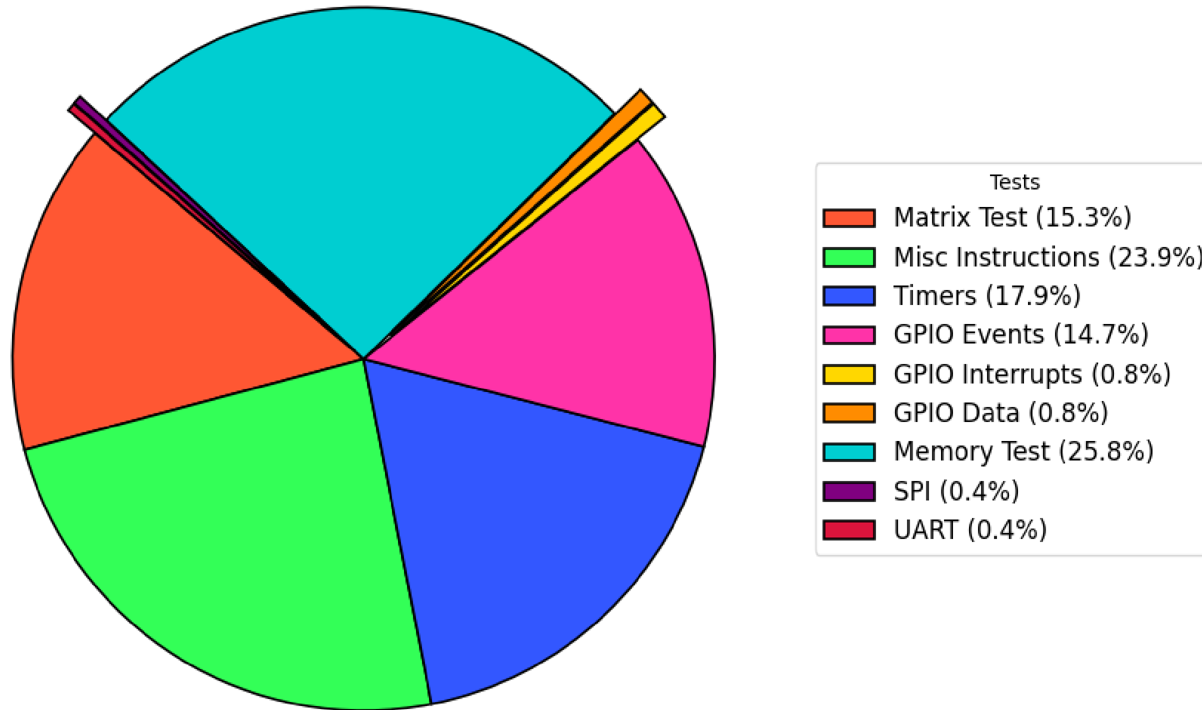


Overall Device SEFI Cross-Section & DBU Cross-Sections Vs. LET

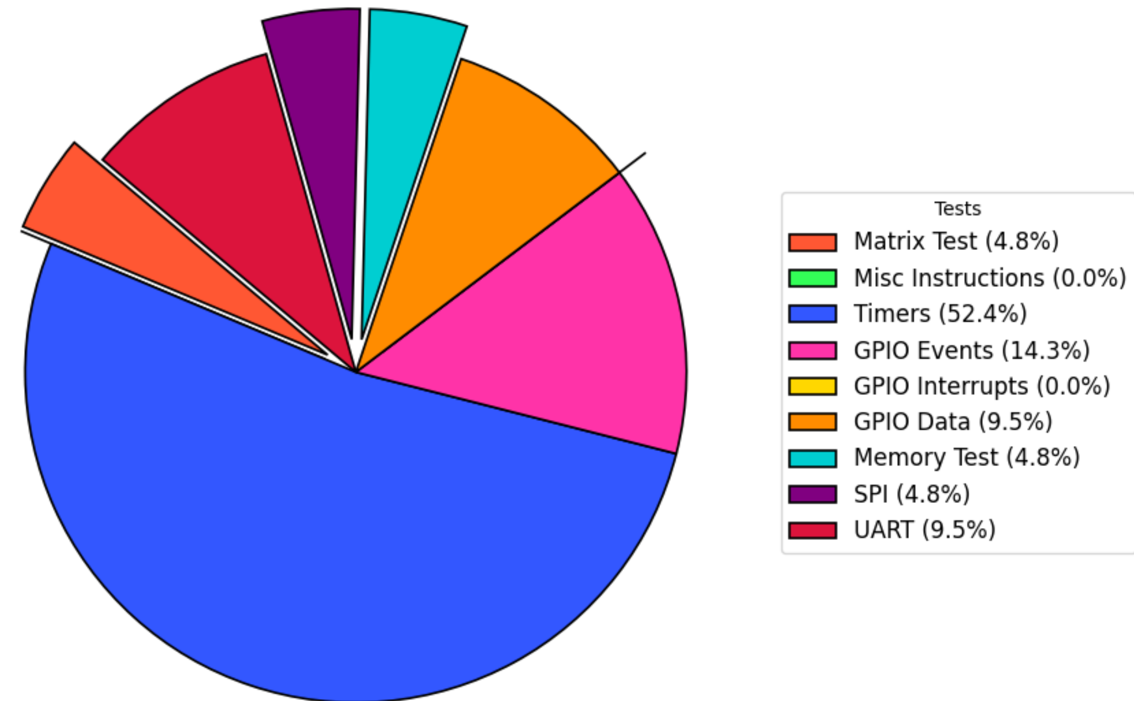


4. Experimental Results – Heavy Ions

Time Taken for Each Unit Test



Percentage of Unit Tests Resulting in SEFIs



4. Experimental Results – Heavy Ions

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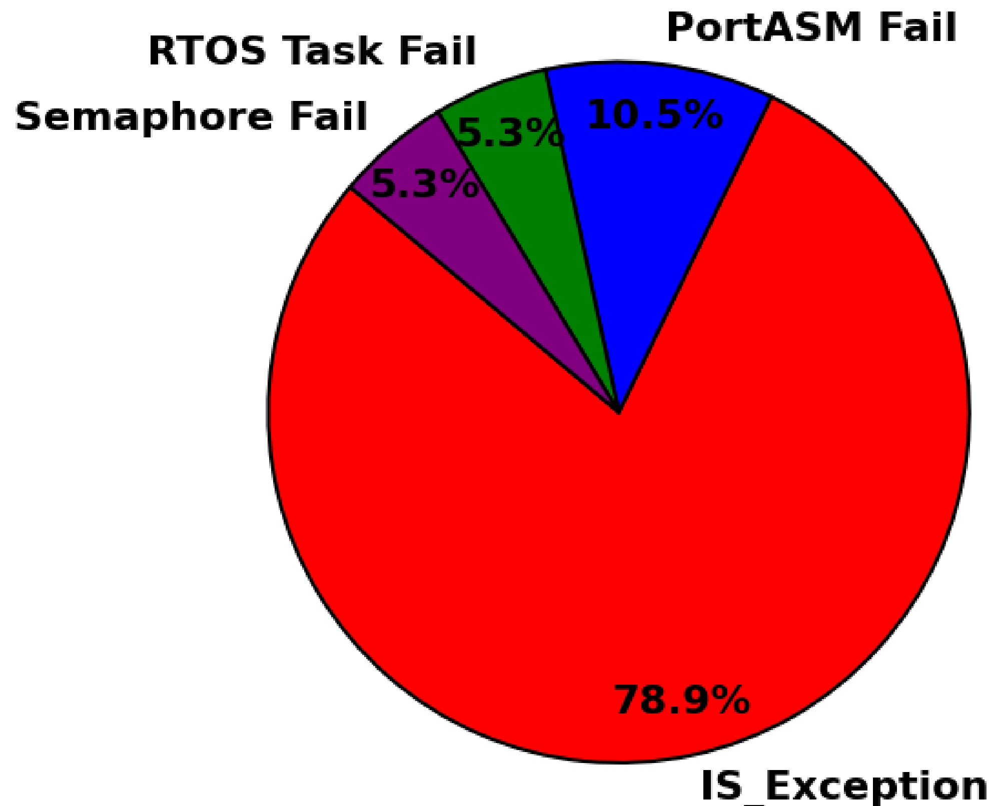
Percent Breakdown of Error Codes Seen



Descriptions of Errors Seen During Testing

Device Error Code	Description & Likely Cause
IS_Exception	Global exception has been raised. Machine program counter, or instruction code is undefined or null.
PortASM Failure	Error during context switching or register service routines. Loaded register values are null or undefined.
Task Control Failure	Priority values for tasks within FreeRTOS are in undefined or null state
Semaphore Failure	Queue pointer in FreeRTOS is in a undefined or Null state.

5. Concluding Remarks – Experiments Summary

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- **Proton Testing:**
  - No failures for either testing mode
  - Very few memory errors
  - TID tolerance up to 200 kRad
- **Heavy Ion Testing:**
  - Failures only for looped testing at every LET
  - DBUs occur at every LET, but the SEFI cross-section stays relatively constant
  - Most SEFIs can be related to corrupted device memory

5. Concluding Remarks – Experiments Summary

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- **Device SEFI rate tends to be more dependent on the testing software rather than particle LET**
  - Non-looped testing routinely scrubs active memory space
  - Looped testing allows for accumulated memory upsets
- **This suggests that accumulated memory errors contribute to device failures**
  - The core and peripherals are assumed to be exceptionally hard
- **Understanding the failure rate of the device due to SEUs depends on more than LET**
  - Per bit cross-section
  - Particle flux rate
  - Average memory access time & scrub

5. Concluding Remarks – Future Work

- **We are working on developing a probabilistic model that considers these factors to better predict SEFI rates**

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- **Pulsed Laser injection testing**
- **Microbeam testing at ANSTO**
- **Payload aboard the next gen USask cube satellite**

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- Pulsed Laser injection testing
- Microbeam testing at ANSTO
- Payload aboard the next gen USask cube satellite
- Potential commercialization

Thank You to our Collaborators!