EMSA5: A RISC-V Processor System for Enhanced Functional Safety in Embedded Applications

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The RISC-V RV32 processor system EMSA5 was originally designed to meet the stringent requirements of functional safety as specified by ISO26262. It consists of a redundant architecture that supports advanced safety mechanisms such as Dual-Mode-Redundancy with Lockstep (DMR-L) and Triple-Mode-Redundancy (TMR), ensuring high reliability in critical applications. However, functional safety is also highly relevant in industrial, avionics and space applications. A comprehensive RISC-V system requires more than just a core; the EMSA5 includes a complete ecosystem tailored for software development, as well as essential peripherals for both processing and communication.

Microprocessor Features

- RV32 RISC-V processor with 5-stage pipeline
- **Redundancy options: DMR-L, TMR**
- Privilege Modes M+U
- PMP for memory access protection
- NMI for handling hardware faults
- Optional vector extensions Zvex32
- Optional FPU (single and double precision)
- Low-power and low-footprint design
- Extensive AMBA based infrastructure
  - AHB-lite, APB
  - Bus protection (Parity and ECC)
- Memory protection by ECC

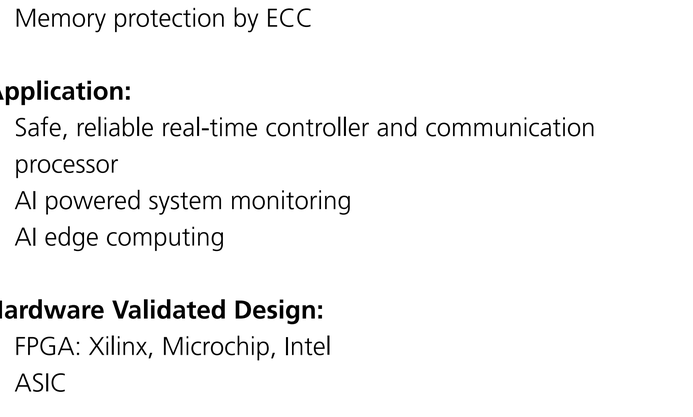
Application:
- Safe, reliable real-time controller and communication processor
- AI powered system monitoring
- AI edge computing

Hardware Validated Design:
- FPGA: Xilinx, Microchip, Intel
- ASIC

Means of Reliability

EMSA5 was originally designed to meet the stringent requirements of functional safety as specified by ISO26262.
- Processor subsystem redundancy, DMR-L, TMR
- Watchdogs
- EDC (Error detection and correction) scheme in bus logic
- ECC protected memories
- Observability by trace interface
- Safety Test Library (STL)

Reliable System by Redundancy and Error Detection and Correction



	Technology	Resources
EMSA5-GP	FPGA[2]	LUTs: 4385, FFs: 2142
EMSA5-FS[1]	FPGA[2]	LUTSs: 15949, FFs: 7717
EMSA5-GP	180 nm	0.217mm², 21.6k ND2gates
EMSA5-FS[1]	180 nm	1.003mm², 100k ND2gates

Minimal configuration, RV32EC
1) Xilinx Artix7
2) TMR, ECC enabled

Ecosystem

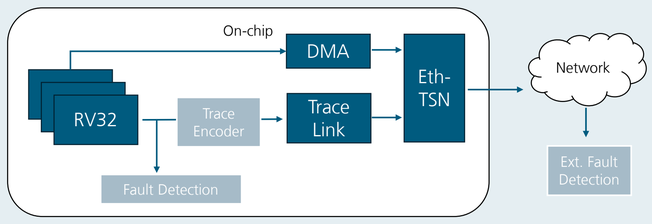
Support for Gnu Compiler Collection (GCC), IAR Embedded Workbench, Lauterbach uTrace, FreeRTOS.

Robustness by Observability

The EMSA5 trace interface significantly increases system robustness due to software verification, fault detection and software verification.

The TraceLink over TSN allows sharing an interface for trace and application data using deterministic TSN features.

TSN Trace Link for Observability

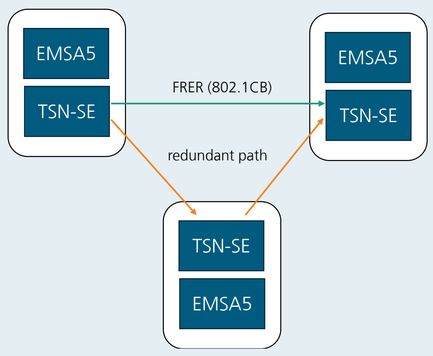


Communication IP Portfolio

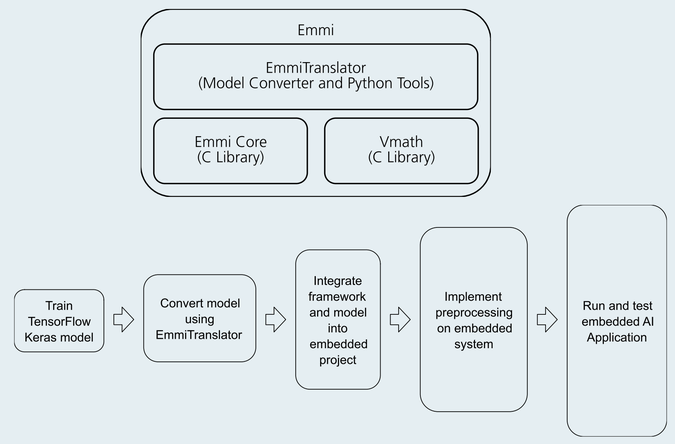
EMSA5 includes a complete ecosystem tailored for software development, as well as essential peripherals for both processing and communication. To facilitate different communication interface requirements, EMSA5 covers both classic CAN and modern Ethernet-based network architectures, demonstrating its versatility in various automotive and industrial applications.

Available IP for communication:
- UART, I2C, SPI
- LIN, CAN – also offered with **redundancy** option
- LLEMAC-1G – Ethernet low-latency MAC with redundancy option
- TSN-EP/SW – Gigabit Ethernet with determinism by TSN Standards
  - 802.1AS for sub-microsecond Time Synchronization
  - 802.1Qav/Qbv – traffic shaping and scheduling
  - 802.1CB – **redundant communication** (FRER)
- Ethernet 10G – offering high speed communication

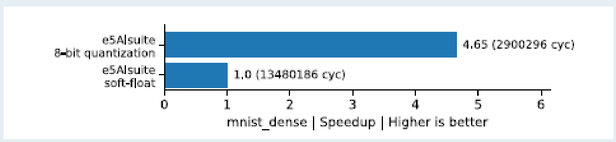
Redundant Data Communication Using FRER (Frame Replication and Elimination)



AI Framework Emmi Components and Workflow



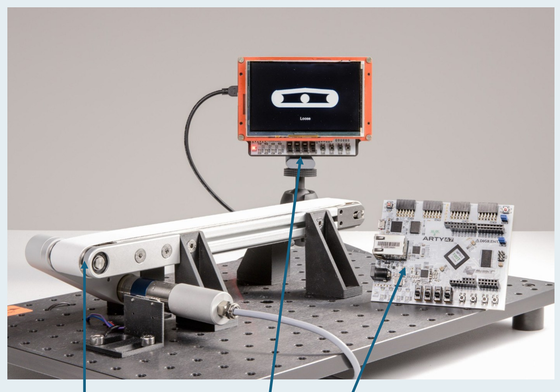
AI Framework Results



Embedded AI Framework

Embedded AI is the name for a field of technologies dealing with artificial intelligence on embedded systems.
Emmi is an inference-only AI framework designed to run neural networks on embedded systems. It offers a layer-based interface for neural networks and is completely written in C. It supports floating-point and integer operations with quantized weights, biases and feature-maps. Models for Emmi are converted from TensorFlow Keras, while sequential and functional models are supported.
The framework has been used in a predictive maintenance application.

Demo setup of the conveyor predictive maintenance application



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