SweRISC PISCES - A Swedish RISC-V Processor in Silicon Carbide for Extreme Space Environments

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For future space exploration both ESA and NASA have selected the RISC-V processor. The RISC-V offers an open instruction set architecture (ISA), meaning that anyone can build a RISC-V without paying royalty. KTH has experience in silicon carbide (SiC) integrated circuit design, with demonstrations of both high temperature operation and radiation hardness. This makes it possible to add radiation hard RISC-V processors through choice of material for space environments. In this paper, we will outline the steps needed to demonstrate a RISC-V processor in SiC for extreme space environments.

1 Background and Relevance to Space Activities

In recent years, ESA and NASA have taken on new challenges in space exploration. In 2023, ESA JUICE (Jupiter Icy Moons Explorer) was launched on an eight-year journey to Jupiter, with a swing by Venus. It is expected that this spacecraft will experience temperatures from -230 to +250 ºC. Once at Jupiter, it will be exposed to large amounts of cosmic radiation. The ESA/NASA Solar Orbiter will come closer to the Sun than ever before and has been tested for temperatures up to 500 ºC. These missions demand more from the spacecraft than ever before.

All spacecraft, from the first Sputnik in 1953, have had electronics on board. Powerful computers have been used to store measurement data and send them back to Earth, and control the spacecraft in its carefully planned orbits. New technologies have been used in space exploration from early on. Microelectronics received a major boost when NASA ordered integrated circuits for the Apollo program's lunar landing computers.

The exploration of space requires careful testing of all the spacecraft's systems, including the electronics and software. Previously tested electronics that have flown in space are often used again because they are known to work (flight-proven). For many years, ESA have used the SPARC (Scalable Processor Architecture) architecture in the computers, which Sun Microsystems developed in the 1980s [1]. Its architecture is completely open, non-proprietary, and royalty-free, which led several companies to use it for space processors. Among them is Cobham Gaisler (now Frontgrade Gaisler) [2] in Gothenburg with its family of LEON processors developed in projects with ESTEC [3].

The advantage of an open, non-proprietary and royalty-free architecture is that anyone can build their own computer, with the intention of improving performance in some way. For spacecraft, it is usually about increasing radiation resistance and expanding the temperature range where the processor works. The LEON architecture is fault tolerant and detects single-event upsets (SEUs) with error-correcting codes and partial redundancy. So far, all of these space processors have been manufactured in radiation-hard silicon processes.

In 2022, NASA decided to invest in RISC-V as a new processor architecture [4], but ESA already started work 2019 [5, 6]. RISC-V is an open and royalty-free instruction set architecture (ISA) [7], which means that whoever wants to use it can choose the architecture freely with respect to pipeline, redundancy, error correction and which subset of instructions to include. In addition to the space industry, a large number of companies has adopted RISC-V: Amazon, Apple, Google, Microchip, Nvidia, Qualcomm, Rambus, Samsung, SiFive, Western Digital and others [8]. In 2023 the The RISC-V Software Ecosystem (RISE) project was formed to make open development tools for the software [9].

Since the SPARC architecture was developed, the semiconductor field has also changed. Nowadays, there is commercial manufacturing of components in the wide bandgap semiconductors silicon carbide (SiC) for high voltage components [10]. Several universities including KTH [11], TU Delft [12] and the University of Arkansas [13], companies such as Raytheon [14], research institutes such as Fraunhofer in Erlangen [12] and NASA Glenn [15] have demonstrated integrated circuits in SiC that can withstand 400 – 800 ºC use. KTH [16], Hiroshima University [17] and companies like Wolfspeed [18] in the USA have shown much higher radiation resistance (10 – 100 times better than silicon) for SiC devices and circuits.

It is now time to build a RISC-V in SiC. It will withstand higher temperatures and more radiation than silicon, thus preparing spacecraft for even more challenging space missions. Our technology development includes the design and production of transistors and circuits for our process design kit (PDK) that includes a standard cell library [19]. We will define a processor in Verilog, test it on an FPGA, and transfer the design to lithographic masks, so that a SiC processor can be manufactured in the SweRISC PISCES project.

2 Methodology

Both ESA and NASA have selected the RISC-V core for future processor applications in space. However, their decision is based on using a standard or radiation hardened silicon process. The SweRISC PISCES project proposes building a silicon carbide (SiC) demonstrator of a RISC-V core for future extreme space environments. KTH SiC integrated circuits have already been shown to withstand temperatures in the 600 °C range [11] as well as radiation hard environments [16]. Other groups have shown high temperature integrated circuits [12-15] and radiation hardness [17].

So far most attempts at integrated circuits in SiC have stopped at a level of 5K – 10K transistors. A minimum RISC-V can be made with less than 20K gates [20], and with a conversion rate of 4 – 6 transistors per gate this equals about 100K transistors. For program and data memory, a minimum memory of about 100K transistors would be reasonable, resulting in 2 kibibytes memory, or 512 words of 32 bit length if we assume 6 transistors per bit. Therefore, we need to aim for 200K transistors in our process design kit.

Objectives and Goals
The over-arching goal of SweRISC PISCES is to demonstrate a RISC-V processor with memory in Silicon carbide (SiC). This poses the following challenges to the project group:

- Design and simulate devices and integrated circuits in SiC
- Develop process technology that can integrate enough transistors for a RISC-V and memory, including exploring self-aligned technologies

- Develop a process design kit that can take Verilog code and generate lithography masks
- Select and design a reasonable size RISC-V processor core that follows the ISA, and select test programs that fit in the minimal memory available
- Process several batches of integrated circuits, and characterize them at high temperatures in a probe station, including running test programs

It should be noted that we already have the basic process technology for logic devices and integrated circuits [19]. All process equipment is already available in the in-house clean room. We see that we are at a stage where the next logical step is to demonstrate integrated circuits corresponding to popular architectures for space exploration. We foresee radiation hardness and high temperature operation, thanks to the use of SiC.

In previous experiments we have evaluated both bipolar and CMOS transistor technologies at KTH. The bipolar technology has been deemed too power hungry [19], and difficult to scale to the level needed for the RISC-V processor. CMOS technology suffers from threshold voltage variations for p-channel devices, as well as lack of self-alignment techniques for scaling [13, 14, 21]. Other groups have investigated JFET technologies (either normally on or normally off). We suggest an NMOS technology that only uses n-channel transistors, which can be scaled thanks to the use of self-alignment. However, instead of p-channel transistors an alternative pull-up circuitry is required, for instance an enhancement load, depletion load or a resistor [22].

3 Experimental Details

The KTH MyFab Electrum Laboratory is an outstanding resource for fabrication and characterization in the nano and micro scale, supporting the whole chain from education, research and development, to prototyping and production using ISO 9001 certified processes. Complete processes for device and circuit manufacturing have been developed over thirty years by researchers at KTH Electronics, today offering 100 – 200 mm Si CMOS processes as well as the 100 mm SiC bipolar process technology. Some unit processes like SiC epitaxy and ion implantation are routinely purchased from external vendors rather than being maintained in a university environment. This infrastructure is continuously being updated to the users' needs, and we foresee no equipment investments necessary. A complete list of facilities can be found at www.electrumlab.se [23]. There is also state-of-the-art instrumentation for precision DC, RF and low noise electrical characterization of devices and high speed operation of analog and digital circuits available, even up to temperatures of 600 °C. This clean room was selected to fabricate the bipolar SiC devices (BJT and IGBT) for up to 15 kV breakdown voltage in the fourth pilot line of Chips JU [24]. During this phase the SiC line will be upgraded to 150 mm.

4 Conclusions

ESA and NASA has selected RISC-V for future space applications. Radiation hardness has always been a challenge for space exploration, and lately extended temperature ranges have come of greater interest. The wide bandgap semiconductor Silicon carbide (SiC) offers to be a game changer, being inherently radiation hard. KTH has previously demonstrated integrated circuits, but with RISC-V the development can target processor architectures that can be easily exploited by space industry and see wider application.

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